Physical and electrical properties of a Si₃N₄/Si/GaAs metal–insulator–semiconductor structure

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(Received 16 April 2001; accepted for publication 20 July 2001)

We simulated capacitance–voltage (C–V) curves of Si₃N₄/GaAs, Si₃N₄/Si and also Si₃N₄/Semi* (virtual semiconductor) metal–insulator–semiconductor (MIS) capacitors and compared them with experimental C–V curves of a Si₃N₄/Si/GaAs structure. The experimental C–V curves of the Si₃N₄/Si/GaAs MIS capacitors are not in agreement with the simulated C–V curves of the Si₃N₄/GaAs and Si₃N₄/Si MIS capacitors, but are in agreement with those of the Si₃N₄/Semi* MIS capacitors, where Semi* is a virtual semiconductor with $n_i = 7 \times 10^{11} \text{cm}^{-2}$ or $E_G = 0.88 \text{eV}$. This indicates that the Si₃N₄/Si/GaAs structure is somewhat like a narrow band gap material with $E_G = 0.88 \text{eV}$. The comparison yields strong support for our theoretical energy band of the Si₃N₄/Si/GaAs MIS structure based on quantum well confinement. A depletion mode MIS field-effect-transistor (MISFET) is successfully fabricated with transconductance of 85 mS/mm, and an inversion mode MISFET is fabricated with transconductance of 0.05 mS/mm. The small transconductance for the inversion mode MISFET is ascribed to strong scattering due to confinement of electrons in the Si quantum well. © 2001 American Institute of Physics. [DOI: 10.1063/1.1403683]

I. INTRODUCTION

It is the ideal interface between an insulator (SiO₂) and Si that has made the Si complementary metal–oxide–semiconductor (CMOS) the mainstream technology in today’s very-large-scale-integrated (VLSI) circuits. Because of the lack of such an ideal interface between insulators and GaAs, there has never been success in realizing a GaAs based CMOS [or complementary metal–insulator–semiconductor (CMIS)] VLSI circuit. Numerous attempts have been made to passivate the GaAs or InGaAs surface so that an ideal interface could be obtained between insulators and GaAs or InGaAs.¹–¹⁰ However, only two approaches show some promise. One is Si interlayer passivation at the Si₃N₄/GaAs interface.⁹–¹² Using this approach, an interface trap density as low as $5.5 \times 10^{10} \text{cm}^{-2} \text{eV}^{-1}$ on p-GaAs has been achieved.⁹ An n-channel depletion mode MIS field-effect transistor (MISFET) with high transconductance has also been demonstrated using this approach.¹⁰ Another approach is the in situ deposition of Ga₂O₃ on GaAs.¹³–¹⁶ Although the Ga₂O₃/GaAs structure exhibited very low interface trap density in the midgap, larger frequency dispersion might imply a larger trap density near the conduction band as shown in C–V curves in Ref. 14. This is also confirmed by the poor transconductance (0.1 mS/mm⁻¹) of the inversion mode n-channel GaAs MISFET using Ga₂O₃ as the gate insulator.¹⁶ In comparing these two approaches, neither one has a significant advantage over the other regarding surface passivation. It is still significant to study passivation of GaAs using the Si interlayer, which may have wide applications for passivation ranging from FETs, high electron mobility transistors (HEMTs), and metal–semiconductor FETs (MESFETs) to optical devices.

In 1997, collaborating with several co-workers, we calculated the band structure of the Si₃N₄/Si/GaAs system.¹⁷ It was found that the band structure of a strained Si interlayer is very different from its bulk counterpart. Due to the conduction band split, the band gap of the strained Si is only 0.34 eV, much smaller than that of the bulk Si (1.1 eV).¹⁷ In the Si₃N₄/Si/GaAs system, the combination of the strained Si interlayer with Si₃N₄ and wide-band gap GaAs forms a quantum well. The confined energy levels were calculated¹⁷ and are shown in Fig. 1. It was found that the lowest confined energy level in the conduction band is 0.22–0.28 eV above the conduction band edge of the strained Si or 0.57–0.61 eV below the conduction band edge of GaAs. The confined energy level in the valence band is barely above that of GaAs. However, there is no strong experimental evidence to support the above theoretical calculation. The purpose of this article is to present extensive experimental results and simulated results to confirm the above theoretical calculation. Fabrication and characterization of both inversion mode and depletion mode n-channel MISFETs will also be presented.

II. EXPERIMENT

An ultrahigh vacuum (UHV) chemical vapor deposition (CVD) system, connected to a Perkin-Elmer molecular beam epitaxy (MBE) system through a transfer tube maintained at $2 \times 10^{-9} \text{Torr}$, was employed to grow the Si₃N₄/Si/GaAs structure. The background pressures of both the CVD and MBE chambers were maintained at ultrahigh vacuum ($\sim 10^{-9} \text{Torr}$) prior to growth. First, a p-GaAs layer with a
doping level ranging from 3 to $8 \times 10^{16} \text{cm}^{-3}$ was grown on (100) $p^+$-GaAs substrates. Prior to GaAs growth, reflection high energy electron diffraction (RHEED) was used to monitor the thermal cleaning ($T_s \sim 610^\circ \text{C}$) of the substrate surface, which affects the initial stages of epitaxial growth. After GaAs layer growth, the samples were transferred to the UHV CVD chamber without exposure to air. In the CVD chamber, SiH$_4$ and He were introduced into the chamber after the substrate temperature reached 350 $^\circ \text{C}$. A Si interlayer ($\sim 10 \, \text{Å}$) was grown at plasma power of 60 W. By using remote plasma, the surface was kept away from the plasma region, thus reducing any damage caused by energetic particles. A Si$_3$N$_4$ layer ($\sim 200 \, \text{Å}$) was subsequently deposited at 250 W and 350 $^\circ \text{C}$. After growth, the sample was annealed by rapid thermal annealing (RTA) at 550 $^\circ \text{C}$ for 30 s. Finally, 1200 Å thick aluminum was thermally evaporated on the top of the sample and patterned by photolithography to form metal–insulator–semiconductor capacitors with diameters of 300 $\mu\text{m}$. High frequency capacitance–voltage ($C$–$V$) measurements were carried out on an HP 4284A precision low capacitance resonance (LCR) meter, and quasistatic $C$–$V$ measurements were performed on an HP 4140B pA meter/dc voltage source with a ramp rate of 10 mV/s scanned from positive to negative bias.

### III. RESULTS AND DISCUSSION

Section III is organized as follows. First, we present electrical characterization of the MIS capacitors based on $p$-type GaAs. Next, we compare the experimental $C$–$V$ curves with the calculated $C$–$V$ curves of the Si$_3$N$_4$/GaAs, Si$_3$N$_4$/Si, and Si$_3$N$_4$/Semi* MIS capacitors, where Semi* is a virtual semiconductor with $E_G = 0.88 \, \text{eV}$ or $n_i = 7 \times 10^{13} \, \text{cm}^{-3}$. Finally, electrical properties of MISFETs based on Si$_3$N$_4$/Si/GaAs will be studied. In this article, all the samples are based on $p$-type GaAs MIS structures. The results for $n$-type GaAs can be found in other references, and are similar to those for $p$-type GaAs MIS capacitors.

#### A. Electrical characterization of Si$_3$N$_4$/Si/GaAs structures

Figure 2 shows typical $C$–$V$ curves for the Si$_3$N$_4$/Si/p-GaAs structure. The quasistatic $C$–$V$ (QSCV) curve is very close to high frequency curves (1 kHz and 1 MHz) and dips significantly, indicative of an excellent interface between the insulator and $p$-GaAs. The maximum frequency dispersion of 120 mV is clearly seen by the 1 MHz and 1 kHz curves. Inversion is clearly demonstrated by the QSCV curve. The ideal flat-band voltage (without fixed charges in the insulator) for $p$-GaAs is $-1.32 \, \text{V}$. The experimental curve shifts $+0.77 \, \text{V}$, corresponding to a negative charge density of $1.6 \times 10^{12} \, \text{cm}^{-2}$ in the insulator. The quantitative interface trap density was calculated based on the conductance measurement shown in Fig. 3. Details of the calculation approach based on conductance measurement can...
It can be seen that interface trap density as low as $5.5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ in the midgap is demonstrated based on Si interlayer passivation.

Since the critical component for CMOS integration is the $n$-channel inversion mode MOS transistor, whether or not the actual inversion is achieved is critical for GaAs CMIS technology. The above $C-V$ measurements were conducted in the dark. The minority carrier response time is $\tau_r \approx n_i/1$. For GaAs, $n_i$ is small ($n_i = 1.79 \times 10^6 \text{ cm}^{-3}$). This leads to larger $\tau_r$. Thus even in the quasistatic condition, minority carriers may not fully respond to the signal in the dark. No inversion curve was observed at frequency over 10 Hz. In order to increase the generation rate of minority carriers, the above measurements were also carried out under optical illumination. Figure 4 shows the optically excited inversion on the $\text{Si}_3\text{N}_4/\text{Si}/p$-GaAs MIS structure. It can be seen that inversion has been truly been achieved. Even at 20 Hz, the inversion curve appears. In the accumulation and depletion regimes, the frequency dispersion from 20 Hz to 10 kHz is very small. A little larger frequency dispersion is observed from 10 kHz to 1 MHz. This indicates that only fast interface traps are available after passivation. The above experiments confirm that with Si interlayer passivation it is possible to achieve an excellent interface between $\text{Si}_3\text{N}_4$ and GaAs.

B. Comparison of experimental $C-V$ curves with ideal ones

Since much experimental data for $\text{Si}_3\text{N}_4$/GaAs MIS capacitors have been accumulated, it is necessary to compare these data with ideal $\text{Si}_3\text{N}_4$/GaAs MIS capacitors. For Si MOS capacitors, the experimental $C-V$ curves are in excellent agreement with the ideal $C-V$ curves calculated based on Poisson's equation. If GaAs MIS structures exhibit low interface traps, the experimental $C-V$ curves should be in agreement with the theoretical calculation (simulation) based on solving Poisson's equation. The approach employed here is described in detail in Ref. 21. A simple program with input parameters such as insulator thickness $T_{\text{SiN}}$, doping $N_A$, intrinsic carrier concentration $n_i$, and flat-band voltage $V_{\text{FB}}$ was written to simulate $C-V$ curves.

Figure 5 shows $C-V$ curves of $\text{Si}_3\text{N}_4$/GaAs MIS capacitors obtained by simulation, assuming no interface traps. The experimental curves of the $\text{Si}_3\text{N}_4$/Si/GaAs MIS capacitors are also shown in the plot for comparison. It is a surprise that there is a large discrepancy between the experimental curves and the theoretical curves. This is the first bit of evidence that the underlying physics of the $\text{Si}_3\text{N}_4$/Si/GaAs MIS structure is completely different from those of the $\text{Si}_3\text{N}_4$/GaAs MIS structure. The initial assumption for using Si interlayer to passivate GaAs was that this ultrathin Si layer may not affect other electrical properties of the $\text{Si}_3\text{N}_4$/GaAs structure except for reducing interface traps. The results in Fig. 5 indicate that this thin Si layer does influence the electrical properties and that the $\text{Si}_3\text{N}_4$/Si/GaAs structure is not the same as the $\text{Si}_3\text{N}_4$/GaAs structure. Is this structure similar to $\text{Si}_3\text{N}_4$/Si MIS capacitors?

Figure 6 shows $C-V$ curves of $\text{Si}_3\text{N}_4$/Si MIS capacitors obtained by calculation, assuming no interface traps. The experimental curves of $\text{Si}_3\text{N}_4$/Si/GaAs MIS capacitors are also shown in the plot for comparison. There is still a discrepancy between the experimental curves and the ideal curves. Further
thermore, we compare the experimental band bending of the Si₃N₄/Si/p-GaAs MIS structure with the theoretical band bending of the Si₃N₄/p-GaAs and Si₃N₄/p-Si structures as shown in Fig. 7. It can be seen that the experimental band bending of the Si₃N₄/Si/p-GaAs structure is much smaller than the theoretical band bending of the Si₃N₄/p-GaAs structure and even smaller than that of the Si₃N₄/p-Si structure. These results imply that the behavior of the Si₃N₄/Si/GaAs MIS structure is not a simple Si MIS structure. The properties of the Si interlayer are very different from those of bulk Si. What type of MIS structure is it similar to? We assume a virtual semiconductor material, Semi*, with $n_i = 7 \times 10^{11} \text{ cm}^{-3}$ or $E_G = 0.88 \text{ eV}$, and compare the C–V curves of this virtual material with the C–V curves of the Si₃N₄/Si/GaAs structure (see Fig. 8). It can be seen that the C–V curves of this virtual material (Semi*) are in excellent agreement with those of the Si₃N₄/Si/GaAs structure, indicating that the separation between the conduction band and valence band is 0.88 eV. Neither Si nor GaAs MIS structures can explain the behavior of the C–V curves of the Si₃N₄/Si/GaAs structure. In the theoretical band structure of the Si₃N₄/Si/GaAs MIS capacitors shown in Fig. 1, the separation between the confined energy level $E_c$ and $E_v$ is 0.81–0.87 eV, which is very close to 0.88 eV. Therefore, the results in Fig. 8 strongly support the theoretical calculation performed in Ref. 17.

C. Electrical characteristics of Si₃N₄/Si/GaAs MIS transistors

The ultimate goal of this GaAs MIS project is to fabricate viable GaAs MIS transistors for large-scale integration. Here in Sec. III C, fabrication and characterization of both depletion mode and inversion mode GaAs MISFETs using a nitride/Si interlayer structure will be presented. Figure 9(a) shows the structure of the depletion mode MISFET. Fabrication was started with growth of a 0.1 μm thick n-GaAs channel layer (doping $2 \times 10^{17} \text{ cm}^{-3}$) on a 0.5 μm thick undoped GaAs layer on a semi-insulating GaAs substrate. Then, 0.3 μm thick n⁺-GaAs was grown as the ohmic contact. The n⁺ layer is etched off in the channel region and the source and drain were patterned, as shown in Fig. 9(a). The patterned substrate was cleaned by hot $\text{H}_2\text{SO}_4$, cold $\text{H}_2\text{SO}_4$, and rinsed in de-ionized (DI) water, and then immersed in HCL to remove native oxide. Finally, the sample was rinsed in DI water to form oxide. The GaAs substrate prepared was loaded into the MBE chamber. Thermal desorption was performed by elevating the substrate temperature to 580 °C and having sufficient As flux in the chamber. A $(2 \times 4)$ RHEED pattern was observed. After thermal desorption, the sample was transferred to the CVD chamber via an ultrahigh vacuum $(1 \times 10^{-9} \text{ Torr})$ transfer tube. Then an $\sim 10$ Å Si interlayer and 200 Å Si₃N₄ were grown on the patterned substrate at 300 °C. This $\textit{ex situ}$ growth approach also produces a high quality interface with interface trap density of $9 \times 10^{10} \text{ cm}^{-2}\text{ eV}^{-1}$, which is comparable to the $\textit{in situ}$ growth approach. After growth, the
sample was annealed using RTA at 550 °C for 30 s to obtain the optimum interface. AuGe/Ni/Au (400 Å/100 Å/800 Å) was evaporated and alloyed at 500 °C for 1 min to form the source and drain. After mesa etching, a 1000 Å thick aluminum gate was evaporated.

Figure 9(b) shows a schematic of the structure of the inversion mode MISFET, which would be the key device for CMIS integration. The structure and fabrication of the inversion mode device are very similar to the depletion mode device described above. There are only two regions in the inversion mode device in Fig. 9(b), and they are different from those in the depletion mode device in Fig. 9(a). One is the 0.1 μm n+GaAs channel layer and the 0.5 μm undoped GaAs layer in Fig. 9(a) which are replaced by the 0.5 μm p-GaAs layer with a doping level of 1×10^16 cm^-3 as shown in Fig. 9(b). The other one is the aluminum gate, which should overlap the n+ source and drain in the inversion device in Fig. 9(b).

Electrical characteristics of the depletion mode GaAs MISFET are shown in Fig. 10. The gate length is 6 μm and the device width is 40 μm. The gate voltage varies from −3 to 3 V. Maximum transconductance of 85 mS/mm is obtained. The maximum transconductance g_m max for the depletion MISFET is given by

\[ g_{m\text{ max}} = \frac{W}{L} qN_d n_{i_d}, \]

where \( N_d \) and \( t \) are the doping and thickness of the channel layer and are \( 2 \times 10^{17} \text{cm}^{-3} \) and 0.1 μm, respectively. Given the maximum transconductance \( g_{m\text{ max}} \) and device size \( W/L \), the effective electron mobility \( \mu_n \) can be calculated based on the above equation, yielding \( \mu_n \approx 1600 \text{cm}^2/\text{V} \text{s} \). The mobility calculated is determined by two factors: the quality of the GaAs epilayer and the source and drain contact resistance. The GaAs epilayer is of high quality because the intrinsic mobility of the GaAs epilayer doped at \( 2 \times 10^{17} \text{cm}^{-3} \) according to the Hall measurement is \( \approx 4000 \text{cm}^2/\text{V} \text{s} \). The mobility derived from the transistor transconductance \( (1600 \text{cm}^2/\text{V} \text{s}) \) is significantly smaller than the result from the Hall measurement \( (4000 \text{cm}^2/\text{V} \text{s}) \), indicating that the contact resistance is the major limiting factor for the depletion mode device.

Figure 11 shows \( I_D-V_D \) characteristics of the GaAs inversion mode MISFET. This is, we believe, the first inversion mode MISFET based on a Si3N4/Si/GaAs structure. The gate voltage varies from 0 to 6 V and the drain voltage varies from 0 to 5 V. The saturation drain current is proportional to \( (V_G-V_T)^2 \), which is a characteristic typical of an inversion mode MISFET. The extrinsic saturation transconductance \( g_{m \text{ sat}} \) is 0.05 mS/mm. The saturation transconductance is given by

\[ g_{m \text{ sat}} = \frac{W}{L} C_\alpha \mu_n (V_G-V_T). \]

The effective mobility can be calculated based on the above equation, yielding \( \mu_n \approx 0.15 \text{cm}^2/\text{V} \text{s} \). The contact resistance of the source and drain may not be fully responsible for this small mobility. This small mobility implies strong scattering from the interface due to confinement of electrons in the Si interlayer. Because the thickness of the Si interlayer is \( \approx 10 \) or even \( \approx 4 \) Å, inversion electrons in the Si quantum well suffer strong scattering from the interface, resulting in very small electron mobility. This result supports our theoretical calculation shown in Fig. 1 and in Ref. 17.

**IV. CONCLUSIONS**

We simulated \( C-V \) curves of Si3N4/GaAs, Si3N4/Si, and also Si3N4/Semi* (virtual semiconductor) MIS capacitors and compared them with experimental \( C-V \) curves of the Si3N4/Si/GaAs structure. The experimental \( C-V \) curves of the Si3N4/Si/GaAs MIS capacitors are not in agreement with the simulated \( C-V \) curves of the Si3N4/GaAs and Si3N4/Si MIS structures, but are in agreement with those of the Si3N4/Semi* structure, where Semi* is a virtual semiconductor with \( n_i = 7 \times 10^{17} \text{cm}^3 \) or \( E_G = 0.88 \text{eV} \). This indicates that the Si3N4/Si/GaAs structure is somewhat like a narrow band-gap material with \( E_G = 0.88 \text{eV} \). The comparison provides strong support for our theoretical energy band of the Si3N4/Si/GaAs MIS structure based on quantum well
confinement published in Ref. 17. Fabrication and characterization of both depletion mode MISFETs and inversion mode MISFETs are studied. The depletion mode MISFETs are successfully fabricated with transconductance of 85 mS/mm, and the inversion mode MISFETs are fabricated with transconductance of 0.05 mS/mm. The small transconductance for the inversion mode MISFETs is ascribed to strong scattering due to the confinement of electrons in the Si quantum well.

ACKNOWLEDGMENTS

This research was supported by the National Science Foundation (Grant Nos. ECS-0093156 and DAAR-7809086) and by the University of Kentucky Research Challenge Trust Fund (RCTF).