Fundamental connection between hydrogen/deuterium desorption at silicon surfaces in ultrahigh vacuum and at oxide/silicon interfaces in metal–oxide–semiconductor devices

Kangguo Cheng and Jinju Lee
Beckman Institute for Advanced Science and Technology, University of Illinois at Urbana-Champaign, 405 North Mathews Avenue, Urbana, Illinois 61801

Zhi Chen
Department of Electrical Engineering, University of Kentucky, Lexington, Kentucky 40506

Samir A. Shah, Karl Hess, Jean-Pierre Leburton, and Joseph W. Lyding
Beckman Institute for Advanced Science and Technology, and Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, 405 North Mathews Avenue, Urbana, Illinois 61801

(Received 28 February 2001; accepted 21 May 2001)

The fundamental connection between electron stimulated desorption (ESD) of hydrogen (H)/deuterium (D) at silicon surfaces in ultrahigh vacuum and hot-carrier-stimulated desorption of H/D at the oxide/silicon interfaces in complementary metal–oxide–semiconductor (CMOS) devices is presented. The dependences of device degradation on carrier energy and current density were studied on two generations of CMOS devices. The results suggest that the interface degradation in long channel devices is primarily due to the desorption of H/D by high energy electrons through the direct electronic desorption mechanism, while the multiple vibrational heating mechanism becomes important for ESD of H/D in deep submicron devices. By measuring interface trap generation at various stressing conditions in large time scales, we also provide experimental evidence to show that, unlike the uniform energy distribution of Si–H on silicon surfaces, the disordered interface environment introduces a variation of Si–H bond strength at the interface. © 2001 American Vacuum Society. [DOI: 10.1116/1.1385687]

I. INTRODUCTION

The fundamental scanning tunneling microscopy study on the desorption of hydrogen (H) and deuterium (D) on silicon in ultrahigh vacuum (UHV) led to the discovery of the giant H/D isotope effect. Deuterium was found to be much more difficult to desorb than hydrogen. This discovery inspired the idea of using deuterium to improve the hot-carrier lifetime of complementary metal–oxide–semiconductor (CMOS) devices. The improvement has been attributed to the high resistance of Si–D bonds to the bombarding of channel hot carriers. Nevertheless, due to the complex interface environment and the nonuniform spatial and energy distributions of channel carriers, the desorption mechanism at the interface is far more complicated than at silicon surfaces. It is also worthy noting that, given the highly disordered environment of the interface between amorphous gate oxide and single-crystal silicon substrate, Si–H(D) bonds at the interface may not necessarily have the same bond strength. This is different from the Si–H(D) bonds at the silicon surface where all bonds have the same energy. Unfortunately, the uniform bond strength assumption, which assumes the Si–H bond energy (~3.6 eV) to be the threshold energy barrier for H/D desorption at the interface, has generally been used in the hot-carrier degradation model. According to the uniform threshold energy assumption and diffusion-limited degradation theory, the time dependence of device degradation has been proposed to follow the power law, \[ \Delta D = At^n, \] where \( \Delta D \) represents the degradation of any device performance parameter and \( A \) is a constant for a given stressing condition and device structure. The power factor \( n \) is often found to be close to 0.5 for long channel MOS devices. Nevertheless, significant hot-carrier degradation has been observed in deep submicron MOS devices even when they were stressed at voltages lower than 3.6 V. Moreover, the dependence of device degradation on the stress time has also been found to be well below \( t^{0.5} \). These findings impose a serious challenge to the well-defined uniform threshold energy theory and the power law relationship. To resolve this controversy, Hess et al. proposed that the bond energy of some Si–H bonds at the interface might be substantially lower than 3.6 eV.

In this article, we first elucidate hot-electron-stimulated H/D desorption mechanisms at the interface by investigating the stress voltage dependence of the isotope effect in two generations of MOS devices with the different gate lengths. We then present the experimental evidences that support the Si–H bond strength variation theory.

II. DEVICES AND EXPERIMENTS

The devices used in this study were fully processed \( n \)-channel MOS devices fabricated by two different genera-
tions of CMOS technologies. The channel length \( L \) for the long channel devices was 0.35 \( \mu \text{m} \) at the mask level with the gate oxide thickness of 55 Å. For the short channel devices \( L \) was 0.18 \( \mu \text{m} \) and the gate oxide thickness 35 Å. After deposition of the interconnection metal layers, all devices were annealed in hydrogen or deuterium at 450 °C for 3 h to passivate the silicon dangling bonds at the oxide/silicon interface. Desorption of H/D at the interface of these devices were achieved by monitoring interface trap density \( (N_{it}) \) evolution under various channel hot electron stress. \( N_{it} \) was measured by the charge-pumping technique. All electrical tests were performed at room temperature and controlled by an HP4155A semiconductor parameter analyzer.

### III. RESULTS AND DISCUSSION

#### A. Gate-voltage dependence of H/D isotope effect

Figure 1 shows channel-hot-electron stimulated interface trap creation in two types of devices with different gate lengths. For each generation of devices, the drain stress voltage \( V_{ds} \) is fixed and the gate stress voltages \( V_{gs} \) vary from the threshold voltage \( V_t \) to \( V_{ds} \). Interface trap generation in these two types of devices exhibits opposite dependences on \( V_{gs} \). For the long channel devices \( (L = 0.35 \mu \text{m}) \), Fig. 1(a) shows that the worst interface degradation occurs at the lowest \( V_{gs} \) \( (V_{gs} = V_t = 0.5 \text{ V}) \). In contrast, Fig. 1(b) shows that the worst interface degradation occurs at the highest \( V_{gs} \) \( (V_{gs} = V_{ds} = 2.5 \text{ V}) \) in the short channel devices \( (L = 0.18 \mu \text{m}) \). Note that the long channel devices were stressed at \( V_{ds} = 3.75 \text{ V} \) and the short channel devices were stressed at \( V_{ds} = 2.5 \text{ V} \). Such opposite \( V_{gs} \) dependences can be explained by conceivably drawing analogy between electron stimulated desorption (ESD) of H/D at silicon surfaces in UHV and channel-hot-electron stimulated desorption of H/D at the oxide/silicon interfaces.  

![Figure 1](image1.png)

**Fig. 1.** Interface trap creation in deuterated \( n \)-channel devices under various \( V_{gs} \) stress. (a) \( L = 0.35 \mu \text{m}, V_{ds} = 3.75 \text{ V} \); (b) \( L = 0.18 \mu \text{m}, V_{ds} = 2.5 \text{ V} \). Note that for \( L = 0.35 \mu \text{m} \), interface degradation is reduced as \( V_{gs} \) increases, whereas for \( L = 0.18 \mu \text{m} \), it is enhanced as \( V_{gs} \) increases.

![Figure 2](image2.png)

**Fig. 2.** Schematics of the mechanisms of electron stimulated desorption of H/D. (a) Direct electronic excitation: H/D desorption is due to the excitation of Si–H/D from the bonding state to the antibonding state by high-energy electrons. The desorption yield for the electronic excitation mechanism is strongly dependent on electron energy, but independent of the current density. (b) MVH mechanism: H/D desorption is due to the successive excitation of Si–H(D) bonds by multiple electrons with low energy. A competing cooling process due to the coupling between the Si–H(D) bonds with the silicon phonon is also shown. The desorption yield for MVH mechanism is highly dependent on the current density.
been proposed for ESD of H/D at silicon surfaces. In the direct electronic excitation mechanism [Fig. 2(a)], each individual high-energy electron can excite a Si–H(D) bond from the bonding state to the antibonding state, causing H/D desorption. The desorption yield through this mechanism is dependent on electron energy, but independent of the current density. The other mechanism is the multiple carrier vibrational heating mechanism [Fig. 2(b)], in which Si–H(D) bonds are successively excited by multiple electrons with low energy. The desorption yield in this mechanism is dependent on electron energy and the current density.

For the long channel devices stressed at high \( V_{ds} \) (\( V_{ds} = 3.75 \) V), the energy of some channel electrons are high enough to excite H/D from the bonding state to the antibonding state, resulting in the desorption of H/D and therefore the generation of interface traps. The increase of \( V_{gs} \) primarily causes the decrease of channel electron energy due to the reduced maximum electric field \( E_{\text{max}} \) at the high \( V_{gs} \) as indicated by Eq. (1):\(^{20}\)

\[
E_{\text{max}} = \frac{V_{ds} - \varepsilon_{\text{sat}}(V_{gs} - V_f)}{\varepsilon_{\text{sat}}L + (V_{gs} - V_f)} / l,
\]

where \( \varepsilon_{\text{sat}} \) is the electric field when channel electrons reach the saturation velocity, \( L \) is the drawing channel length, and \( l \) is the characteristic length associated with the oxide thickness and the source/drain junction depth. For the direct electronic excitation, the H/D desorption yield decreases with the decrease of the electron energy.\(^{1} \) Therefore, high \( V_{gs} \) stress results in the reduced interface degradation in the long channel devices.

For the short channel devices stressed at a low \( V_{ds} \) (\( V_{ds} = 2.5 \) V), the energy of channel electrons is relatively low, so the multiple vibrational heating (MVH) mechanism may become important for H/D desorption. The MVH mechanism, the desorption yield increases as the current density increases. Based on fundamental device physics, the channel current \( I_{ds} \) increases with increasing \( V_{gs} \) as indicated by Eq. (2):\(^{20}\)

\[
I_{ds} = \frac{W C_{ox} v_{\text{sat}} (V_{gs} - V_f)^2}{(V_{gs} - V_f) + \varepsilon_{\text{sat}}(L - \Delta L)},
\]

where \( W \) is the channel width, \( C_{ox} \) is the gate oxide capacitance, \( v_{\text{sat}} \) is the saturation velocity, \( V_f \) is the threshold voltage, and \( \Delta L \) is the depletions width of the drain. Therefore, the H/D desorption is enhanced at the high \( V_{gs} \) stress for the short channel devices. Figure 3 shows the H/D desorption rate ratio \( \gamma \) as a function of \( V_{gs} \) in these two kinds of devices. \( \gamma \) is defined as the ratio of \( \Delta N_{it} \) between the hydrogenated and deuterated devices after 500 s stress. A total of twelve devices (six hydrogenated and six deuterated) were stressed and the results were averaged for each data point. The error bars indicate the standard deviations. The increase of \( \gamma \) with increasing \( V_{gs} \) for the long channel devices suggests that MVH mechanism may also become important in these devices stressed at the high \( V_{gs} \). For the short channel devices, however, \( \gamma \) decreases with increasing \( V_{gs} \) due to the increase of the current density.\(^{21} \)

State-of-the-art CMOS devices are operated at voltages well below 3 V so that channel carriers do not have sufficient energy to surmount the energy barrier at the oxide/silicon interface. Therefore, device degradation due to charge trapping in the oxide can be significantly suppressed at the lowered operation voltage. However, channel carriers can still desorb H/D through the MVH mechanism. Therefore, interface degradation cannot simply be scaled away by lowering the operation voltages. Instead, interface trap creation may become the dominant device degradation mechanism for deep submicron CMOS devices.

**B. Si–H(D) bond strength variation at the oxide/silicon interface**

Even though the degradation details are still the subject of debate, one of the main degradation mechanisms is interface trap generation due to desorption of hydrogen at the oxide/silicon interface. The degradation process is limited by the diffusion of hydrogen away from the interface.\(^{10} \) The Si–H bond energy (\( \sim 3.6 \) eV) has been assumed to be the threshold energy barrier for hydrogen desorption from the interface. According to this uniform threshold energy and diffusion-limited degradation theory, interface trap generation can be expressed is described by the widely accepted power law\(^{10,11} \)

\[
\Delta N_{it} = N_{it} - N_{it0} = A t^n,
\]

where \( N_{it0} \) and \( N_{it} \) are the interface trap density before and after hot-carrier stress respectively, \( t \) is the stress time and \( A \) is a fitting parameter associated with the stressing conditions. From Eq. (3), the power factor \( n \) can be determined by the expression

\[
n = d \ln \Delta N_{it} / d \ln t.
\]
Figure 4 shows interface trap creation in 0.35 μm n-channel MOS devices stressed at the peak substrate current condition with various drain voltages. From the data in Fig. 4 and Eq. (4), the time dependence of \( n \) is determined and the results are shown in Fig. 5. One can clearly see that, for all stress conditions, \( n \) decreases as stress time increases. The values of \( n \) cover a wide range from \( n \approx 0.8 \) at the initial stress stage to \( n \approx 0.2 \) at the final stress stage. Such a time dependence of \( n \) contradicts to the classical model based on a uniform Si–H bond energy. In the classical model, \( n \) is expected to be a constant around 0.5 and independent of stress time.\(^{11}\)

The power factors extrapolated from the interface degradation data in 0.18 μm devices is shown in Fig. 6. Note that these devices were stressed at the voltages below 3 V, suggesting that the energy for hydrogen desorption from the SiO\(_2\)–Si interface can be significantly lower than 3.6 eV. Again, time-dependent behavior of \( n \) is observed, suggesting that interface degradation of CMOS devices under hot-carrier stress cannot be accurately described by the classical model. Instead, Hess et al.\(^{16}\) proposed that, given the disordered interface between the amorphous gate oxide and the crystalline silicon substrate, there likely is a distribution of Si–H bond energy. While their theory may be debatable, it appears to be the only viable alternative theory at present. The broad distribution of energies could also help explain the continuing degradation of low voltage devices. According to the bond energy variation theory, weaker Si–H bonds with lower energy are more easily broken at the early stress stage. The reason for the sublinear time dependence, i.e., \( n < 1 \), is that weak bonds are broken more rapidly leaving strong bonds to be broken more slowly. The dependence of \( n \) on stress condition and time depends on the detailed nature of the bond and carrier distributions.\(^{22}\) The higher initial values of \( n \) suggests that the tail of the distribution is steeper on a log scale or truncated at lower energy where bonds are broken first.

IV. CONCLUSIONS

The fundamental connection between desorption of H/D at silicon surfaces and at oxide/silicon interfaces has been presented. It is found that multiple heating vibrational mechanism plays an important role for hot-carrier-induced desorption of H/D at the interface in deep submicron devices. Unlike the uniform Si–H(D) bond energy at silicon surface, our experimental results support the hypothesis of Si–H(D) bond strength variation at the oxide/silicon interfaces.

ACKNOWLEDGMENTS

This work was supported by the Office of Naval Research under Grants No. N00014-00-1-0234 and No. N00014-98-1-0604 and the Beckman Institute for Advanced Science and Technology at the University of Illinois at Urbana-Champaign. The authors thank Y.-K. Kim, Y.-W. Kim, and K.-P. Suh at Samsung Electronics for providing the test devices. The authors also thank Ronald Rattray of Spectra Gases Inc. for donating the deuterium used in these experiments.


1123 Cheng et al.: Fundamental connection between hydrogen/deuterium

---