Chapter 3

The Metal Layers

- Bond Pad
- Design and Layout
- Parasitics
- DRC
- Cross Talk, Ground Bounce
Bond Pad

DESCRIPTION
- INTERFACE: CHIP TO WORLD
- ESD PROTECTION
  - NECESSARY
  - MORE DETAILS LATER
- SIZE DEPENDS ON USAGE
  - BOND PAD
    - SIZE SET BY WIRE PROCESS
  - ETEST PAD
    - SIZE SET BY PROBE CARD
  - MICRO PAD
    - SIZE SET BY MICRO-TIP
- LOCATION
  - BOND PAD
    - TOP METAL LAYER
  - ETEST PAD
    - ALL ROUTING LAYERS
  - MICRO PAD
    - ANY ROUTING LAYER
- PASSIVATION
  - MUST REMOVE TO PROBE
  - PAD.DG LAYER USED FOR MASK
Design and Layout

**DESCRIPTION**

- **CONNECTIVITY**
  - METAL1 → VIA1 → METAL2

- **RULES**
  - VIA1 MUST BE ENCLOSED BY
    - METAL1
    - METAL2
  - VIA1 IS ONE FIXED W/L

- **CONNECTIVITY**
  - METAL1 → VIA1 → METAL2
  - NWELL IS NOT CONNECTED
  - HOW TO CONNECT TO NWELL?

- **CAN / SHOULD HAVE MANY VIAS**
  - HOW MANY VIAS IN A DESIGN?

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**Figure 3.4** Layout and cross-sectional views.

**Figure 3.5** An example layout and cross-sectional view using including the n-well.

**Figure 3.15** The schematics of the contact resistances for the layouts in Fig. 3.14.
Parasitics

**DESCRIPTION**
- SEPARATE DEVICE FROM OTHER
  - WHAT DEVICES ARE HERE?
  - WHAT “OTHER” IS HERE?

**RESISTANCE**
- METAL SHEET RHO
  - WHAT ARE UNITS OF SHEET RHO?
  - HOW IS SHEET RHO FOUND?
- VIA RESISTANCE
  - NO SHEET RHO, WHY?

**CAPACITANCE**
- METAL1 OVER SUBSTRATE
  - WHERE ARE TERMINALS?
  - DISTRIBUTED CAP ➔ LUMPED
- METAL2 OVER METAL 1

**DISTRIBUTIONS**
- RESISTANCES, CAPS DO NOT HAVE ONE VALUE ONLY
ELECTROMIGRATION, DRC

DESCRIPTION

- ELECTROMIGRATION
  - LIMITS $I_{\text{max}}$
  - DUE TO BAMBOO FORMATION
  - SEPARATION, FAILURE

- DRC RULES
  - BOOK VALUES ARE NOT TYPICAL
  - NEED DESIGN RULE PRIMER

- TERMINOLOGY
  - ENCLOSURE
  - SPACING
  - WIDTH
  - OVERLAP

KEY PHRASE, THESE ARE NOT THE RULES THAT YOU USE

Figure 3.11 Design rules for the metal layers using the CMOSEDU rules.
Cross Talk, Ground Bounce

**DESCRIPTION**

- **CONDUCTORS INTERACT**
  - EM FIELD OVERLAP, V INDUCED

- **CROSS TALK**
  - AC SIGNALS
  - \( I_{\text{mutual}} = C_{\text{mutual}} \frac{dV_{\text{signal}}}{dt} \)

- **GROUND BOUNCE**
  - AC, DC SIGNALS

- **V=IR**
  - CAUSE AND EFFECT
  - V IS FROM POWER SUPPLY
  - I IS FROM V/R
  - R IS FIXED, BASED ON ROUTING

- **DECOUPLING CAP**
  - STORES VDD CHARGE
  - TRANSIENT CURRENT

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**Figure 3.16** Conductor used to illustrate crosstalk.

**Figure 3.17** Illustrating problems with incorrectly sized conductors.

**Figure 3.18** Estimating the decoupling capacitance needed in an output buffer.