AGENDA (9/01)
- REMINDER: HOMEWORK DUE TODAY
- REMINDER: NEW HOMEWORK ON WEB (DUE 9/8)
- PARTICIPATION BONUS
- RECAP
- BAKER CH3: METAL LAYERS
  • BOND PADS, E-TEST PADS
  • DRC RULES
  • CROSS SECTION WITH METAL
- QUIZ

AGENDA (9/06)
- ACTIVE LAYERS
- ESD
- RESISTORS & CAPACITORS

AGENDA (9/08)
- LAYOUT → CROSS-SECTION PRACTICE
- MOSFET OPERATION
RE-CAP (8/30)

- $R = R_{SH} \times \#\,\text{SQUARES}, \quad \#\,\text{SQ} = L/W, \text{ FOR ANY LAYER}$
- JUNCTION CAPACITANCE
  - CAP VS. VOLTAGE
- TRADEOFF OF THICKER METAL VS. THINNER METAL
- MIN FEATURE SIZE

OTHER POST-CLASS QUESTIONS ASKED

- HOW DO YOU MAKE TRANSISTORS FASTER?
- WHAT’S A SCANNER?
- WHAT DOES RAM STAND FOR IN CY TECHS?
- WHAT’S FOX?
Chapter 3

- The Metal Layers
  - Bond Pad
  - Design and Layout
  - Parasitics
  - DRC
  - Cross Talk, Ground Bounce
PAD INTERFACE TO OUTSIDE WORLD

- BOND PAD → PRODUCT

Figure 4.20 Layout of a padframe using pads with ESD diodes.

- ADVANTAGE OF SMALLER PADS?
PAD INTERFACE TO OUTSIDE WORLD

- E-TEST PAD \( \rightarrow \) DEVICE CHARACTERIZATION
**Bond Pad**

- **DESCRIPTION**
  - INTERFACE: CHIP TO WORLD
  - ESD PROTECTION
    - NECESSARY
    - MORE DETAILS LATER
  - NO DEVICES UNDER PAD
  - SIZE DEPENDS ON USAGE
    - BOND PAD
      - SIZE SET BY WIRE PROCESS
    - ETEST PAD
      - SIZE SET BY PROBE CARD
    - MICRO PAD
      - SIZE SET BY MICRO-TIP
    - SIZE NOT SHRINK W/POLY SHRINK
  - LOCATION
    - BOND PAD
      - TOP METAL LAYER
    - ETEST PAD
      - ALL ROUTING LAYERS
    - MICRO PAD
      - ANY ROUTING LAYER
  - PASSIVATION
    - MUST REMOVE TO PROBE
    - PAD.DG LAYER USED FOR MASK

**WHAT'S MISSING?**
**Design and Layout**

- **DESCRIPTION**
  - CONNECTIVITY
    - METAL1 $\rightarrow$ VIA1 $\rightarrow$ METAL2
  - RULES
    - VIA1 MUST BE ENCLOSED BY
      - METAL1
      - METAL2
    - VIA1 IS ONE FIXED W/L
  - CONNECTIVITY
    - METAL1 $\rightarrow$ VIA1 $\rightarrow$ METAL2
    - NWELL IS NOT CONNECTED
    - HOW TO CONNECT TO NWELL?
  - CAN / SHOULD HAVE MANY VIAS
    - HOW MANY VIAS IN A DESIGN?

**Figure 3.4** Layout and cross-sectional views.

**Figure 3.5** An example layout and cross-sectional view using including the n-well.

**Figure 3.15** The schematics of the contact resistances for the layouts in Fig. 3.14.
Parasitics

- **DESCRIPTION**
  - SEPARATE DEVICE FROM OTHER
    - WHAT DEVICES ARE HERE?
    - WHAT “OTHER” IS HERE?

- **RESISTANCE**
  - METAL SHEET RHO
    - WHAT ARE UNITS OF SHEET RHO?
    - HOW IS SHEET RHO FOUND?
  - VIA RESISTANCE
    - NO SHEET RHO, WHY?

- **CAPACITANCE**
  - METAL1 OVER SUBSTRATE
    - WHERE ARE TERMINALS?
    - DISTRIBUTED CAP → LUMPED
  - METAL2 OVER METAL 1

- **DISTRIBUTIONS**
  - RESISTANCES, CAPS DO NOT HAVE ONE VALUE ONLY
**ELECTROMIGRATION, DRC**

- ELECTROMIGRATION
  - LIMITS $I_{max}$
  - DUE TO BAMBOO FORMATION
  - SEPARATION, FAILURE

- DRC RULES
  - BOOK VALUES ARE NOT TYPICAL
  - NEED DESIGN RULE PRIMER

- TERMINOLOGY – BASIC RULES
  - ENCLOSURE
  - SPACING
  - WIDTH
  - OVERLAP

**KEY PHRASE, THESE ARE NOT THE RULES THAT YOU USE**

[http://www.ifw-dresden.de/ifs/31/gfa/em_e.htm](http://www.ifw-dresden.de/ifs/31/gfa/em_e.htm)
Cross Talk, Ground Bounce

DESCRIPTION
- CONDUCTORS INTERACT
  - EM FIELD OVERLAP, V INDUCED

- CROSS TALK
  - AC SIGNALS
  - \( I_{\text{mutual}} = C_{\text{mutual}} \frac{dV_{\text{signal}}}{dt} \)

- GROUND BOUNCE
  - AC, DC SIGNALS

- \( V=IR \)
  - CAUSE AND EFFECT
  - V IS FROM POWER SUPPLY
  - I IS FROM V/R
  - R IS FIXED, BASED ON ROUTING

- DECOUPLING CAP
  - STORES VDD CHARGE
  - TRANSIENT CURRENT

Figure 3.16 Conduors used to illustrate crosstalk.

Figure 3.17 Illustrating problems with incorrectly sized conductors.

Figure 3.18 Estimating the decoupling capacitance needed in an output buffer.
**DECOUPLING CAP**

Example: 3.9
- Circuit during switching needs 50uA for 10 ns
  - \( I = C \cdot \frac{dV}{dt} \)
- What's size of decoupling cap, to keep \( \Delta V \) below 10 mV?

Solution
- \( Q = I \cdot \Delta t = 50\mu A \cdot 10 \text{ ns} = 500 \text{ fC} \)
- \( Q = C \cdot \Delta V \)
  - \( C = \frac{Q}{\Delta V} = \frac{500 \text{ fC}}{10 \text{ mV}} = 50 \text{ pF} \)

Figure 3.17 Illustrating problems with incorrectly sized conductors.

Figure 3.18 Estimating the decoupling capacitance needed in an output buffer.