Chapter 1

- The CMOS IC Design Process
  - Fabrication
  - Layout and Cross Sections
CMOS Design Flow

- Define circuit inputs and outputs (Circuit specifications)
- Hand calculations and schematics
- Circuit simulations
- Does the circuit meet specs?
  - Yes: Layout
  - No: Re-simulate with parasitics
  - No: Does the circuit meet specs?
    - Yes: Prototype fabrication
      - Test and evaluate
        - No, fab problem
          - Does the circuit meet specs?
            - Yes: Production
            - No, spec problem
          - Test and evaluate
            - No, fab problem
              - Does the circuit meet specs?
                - Yes: Production
                - No, spec problem
  - Yes: Layout

DESCRIPTION
- General Flow
- Block Level Design
- Simulations
  - Schematic vs. Layout
- Usually no prototype
- Need feedback loop to design
- Models implied
Fabrication

- Diameter of Wafer vs. Die size
- View pattern across wafer
  - Printing $\rightarrow$ Reticle
- Die Size vs. Package Size
  - Bond pad limited designs
- Terminology
  - Die – 1
  - Dice – many
  - Most people will use “die” for both

- Read chapter 1 on cross sections
  - Switch between layout, xsect