I. Instructional Objectives

- Analyze the MOSFET transistors as digital devices
- Measure the effect of stray capacitance in MOSFET transistor digital circuits
- Know the nomenclature of digital circuits

See Horenstein 5.2.2, 6.1.2, 6.4.1, and 6.4.2

II. Background

This lab deals with the digital (nonlinear or large signal) operation of MOSFET transistors. The operation of a MOSFET can be understood by plotting the load line (Kirchhoff’s voltage law for the drain circuit) on the characteristic curves of the MOSFET. The MOSFET’s drain-to-source voltage can never be greater than the $V_{DD}$ supply voltage (cutoff region $I_D = 0$) or less than zero (triode region). Digital applications call for the device to be operated at the extreme ends of the transfer characteristic (load line), designated logic 1 for high drain-to-source voltage (cutoff region, $I_D = 0$, $V_{DS} = V_{DD}$) and logic 0 for low output voltage (triode region, $V_{DS} =$ small value, $I_D = $ its maximum value). The region between these two extremes is called the analog region. This region is undefined for digital operation and is traversed only when the output changes between its logic 1 and logic 0 states.

This lab uses the MOSFET transistor in common logic circuits. The simplest logic circuit uses the MOSFET in the common source configuration to perform the logic negate function. This device is referred to as an inverter. The configuration for such an inverter is shown below in Fig. I. Figure 2 shows the circuit’s transfer characteristic, truth table, and truth table in terms of voltage levels. Ideally, the transfer function’s transition from a digital high value to a digital low value will be a vertical line at $V_{DD}/2$ and $V_{OL}$ will be zero. The sharpness of this transition depends on the $Kp$ of the MOSFET, where more vertical transitions result from a higher $Kp$ MOSFET.
It is generally not desirable to use very high $Kp$ MOSFETs in digital circuits, since these devices are physically large and this limits the number of transistors that can be placed on a single chip. The single chip MOSFET used in the lab has an unusually large $Kp$ and is larger than normal digital MOSFETs. The highest output voltage produced by the inverter occurs when its input is a logic zero ($V_{in} \approx 0V$) and its output (with no load) represents logic 1. This voltage is given the symbol $V_{OH}$. If the inverter is fed an input voltage equal to $V_{OH}$, the result is a low output voltage, representing logic 0. This voltage is given the symbol $V_{OL}$. In practice, many effects, including output loading, noise, power supply fluctuations, and component variations will cause extraneous voltage components to be added to or subtracted from the otherwise perfect logic signals $V_{OH}$ and $V_{OL}$. Thus, the input voltage levels the logic circuits must interpret as logic 1 and 0 are usually extended slightly into the analog region to include voltages lying slightly below $V_{OH}$ and slightly above $V_{OL}$. For the case where the output of the logic inverter is 1, the drain current is zero and thus $V_{in} < V_{tr}$. The case for a logic inverter output of 0 is more complex since the MOSFET is operating in the triode region. Recall in the triode region for $V_{GS}=V_{IH}$:

$$I_D = Kp \left( V_{GS} - V_{tr} \right) V_{DS} - \frac{V_{DS}^2}{2} = Kp \left( V_{IH} - V_{tr} \right) V_{DS} - \frac{V_{DS}^2}{2}$$

(1)

When $V_{DS}$ is small the $V_{DS}^2$ term can be neglected (this is the same as expanding the function $I_D(V_{GS}, V_{DS})$ in a Taylor series and keeping only the linear terms) and the drain current can be approximated as:

$$I_D = Kp(V_{IH} - V_{tr})V_{DS} = \frac{V_{DS}}{r_{on}} \text{ where } r_{on} = \frac{1}{Kp(V_{IH} - V_{tr})}$$

(2)

Thus the circuit in Fig. 1 can be approximated with the circuit in Fig 3 when the output is logic 1 and the circuit in Fig. 4 when the output is a logic zero.
III. Pre-Laboratory Exercise

You are to design a logic inverter using the ZVN3306A with $K_p = 2K = 0.1233$ A / V$^2$, and $V_{tr} = 1.8$ V (or 2N7000 N-channel MOSFET with $K_p = 2K = 0.225$ A / V$^2$, and $V_{tr} = 2.1$ V). Or, you can use the values you measured in the last lab if you think they are reasonable. The drain voltage supply is 5Vdc and the drain current with a logic zero output is to be approximately 1 mA.

1. For the MOSFET inverter described above, find $V_{IL}$, which is he largest value that $V_{in}$ can have when the MOSFET is in cutoff mode, with $V_{out} = V_{DD}$ and $V_{in}$ corresponding to logic 0. What is $I_D$ in this case? Does the result depend on $R_D$?

2. Estimate the MOSFET’s channel resistance $r_{on}$ for the ZVN3306A/2N7000 ($V_{GS} = 5$V). Determine $V_{OL}$ when the drain current is 1mA.

3. What must the logic inverter’s drain resistor value be?

4. Using your drain resistor from part 3) draw the circuits load line and at least one device characteristic curve, the one for $I_D = 1$mA. For the MOSFET in saturation mode, determine the gate to source voltage so that the drain current equals 1mA. For this gate to source voltage, what value of drain-to-source voltage is at the boundary between the saturated and triode regions of MOSFET operation?

5. What are $V_{OH}$ and $V_{OL}$ for the MOSFET inverter with no load, a 10kΩ load, and a general MOSFET inverter load $R_{load}$?

6. What is the drain current for logic 1 out and logic 0 out with no load (no load = infinite), a 10kΩ load, and a general MOSFET inverter load $R_{load}$?

7. What is the power from the $V_{DD}$ supply and $V_{in}$ source for logic 1 out and logic 0 out?

8. Simulate your inverter design using SPICE. Use the level 1 model of the MOSFET with the values of $K_p$ and $V_{tr}$ for the ZVN3306A/2N7000 listed above (or the values you measured last lab) and leaving all of the other MOSFET parameters at their default values. Make your own MOSFET model. Do not use the ZVN3306A/2N7000 library model. Make your input a 10kHz pulse (there is a pulse wave form in SPICE) that is 0V for half of the time and 5V for half of the time. Let the rise and fall times equal to 5μs.
Plot the input and output for two cycles and record the time step (Step Ceiling value) you use.

9. Determine the truth tables, as in Fig. 2, for the circuits in Figs. 5 and 6. Determine the numerical values of $V_{OL}$ and $V_{OH}$ with no load ($R_{load} = $ infinite) for each combination of inputs with $V_{IL} = 0V$, $V_{IH} = 5V$, and $V_{DD} = 5V$ using $R_{D} = 5.1k\Omega$ and reasonable approximations.

![Fig. 5. Mystery logic gate circuit](image1)
![Fig. 6. Mystery logic gate circuit](image2)

IV. Laboratory Exercise

1. Construct the MOSFET inverter circuit using the drain resistance value from the pre-lab. Make $R_{G} = 10k\Omega$. Put a 1kHz triangle wave into the input. Measure and record the circuits transfer characteristic. Indicate on your transfer characteristic where $V_{GS}$ equals $V_{tr}$.

2. Experimentally determine $V_{OH}$, $V_{OL}$, and $V_{tr}$. Indicate on your recorded input and output waveforms when $V_{GS}$ equals $V_{tr}$. (Discussion: Compare the measured $V_{OH}$ and $V_{OL}$, to those calculated in the pre-lab. Compare the $V_{tr}$ measured using the inverter circuit to that measured with the curve tracer from the previous lab. Explain differences and similarities.)

3. Make the input a 0V to 5V, 100 kHz square wave. Record $V_{out}$ and $V_{in}$ to demonstrate your circuit inverts the input.

4. Measure the rise time, turn off delay time, the fall time and the turn on delay time defined in Fig. 7. You will have to trigger on the positive edge and then the negative edge of the input voltage and display both $V_{out}$ and $V_{in}$ simultaneously. Expand the waveform using the horizontal time per division adjust. Decrease the time per division until you can observe the rise time, fall time and delay times. Record your waveform for the rise time measurement. (Discussion: Explain differences in the delay times and the rise and fall times.)

5. Measure and record $V_{out}$, $V_{GS}$, and $V_{DD}$ from the power supply.

6. Determine approximately the maximum frequency this inverter can operate at. Record $V_{out}$ at this frequency.
7. Raise $V_{DD}$ (and your input signal) to 10V and repeat parts 3 – 6 (except you do not have to record the waveforms). (Discussion: What conclusions can you draw regarding the effects of $V_{DD}$?)

8. Change $R_G$ to 1k$\Omega$ and again measure the rise time, turn off delay time, the fall time and the turn on delay time with $V_{DD} = 5V$. (Discussion: What conclusions can you draw regarding the effect of $R_G$?)

9. Build the circuits in Figs. 5 and 6. Use your laboratory power supply as the input to the circuit and measure the truth tables, as in Fig. 2. Measure and record the numerical values of $V_{OL}$ and $V_{OH}$ with no load ($R_{load} = infinite$) for each combination of inputs with $V_{IL} = 0V$, $V_{IH} = 5V$, and $V_{DD} = 5V$ using $R_D = 5.1k\Omega$ and $R_G = 10k\Omega$. (Discussion: How do your measured results compare to your calculated pre-lab results.)

Fig. 7. Definitions of delay, rise, and fall time