Reduction of gate leakage current of HfSiON dielectrics through enhanced phonon-energy coupling

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The authors have investigated the effect of phonon-energy-coupling enhancement induced by rapid thermal processing (RTP) and deuterium annealing on the leakage current characteristics of HfSiON gate dielectrics. The leakage current is reduced by one- and-a-half orders of magnitude after RTP and deuterium annealing of HfSiON gate dielectrics. The leakage current density of the HfSiON gate insulator with equivalent oxide thickness of 5.2 Å was only 4×10^{-2} A cm^{-2}. This suggests that HfSiON with the enhanced phonon-energy coupling can be scaled down to below 5 Å. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2363139]

The aggressive scaling and low gate leakage current are required to improve the current drive capability and to reduce standby power in future metal-oxide-semiconductor field effect transistors (MOSFETs).[1] For the above purpose, high-*k* gate dielectrics are extensively studied for the potential replacement of SiO_2 and SiO_xN_y in advanced MOSFETs. One of the most promising high-*k* gate oxides is HfSiON due to its excellent thermal stability, improved electrical properties, and reduced dopant diffuson.[2–4] Recently, we discovered phonon-energy-coupling enhancement (PECE) effect of the SiO_2/Si system, i.e., phonon-energy coupling is enhanced among Si–O, Si–Si, and Si–D bonds, leading to a large reduction of leakage current of SiO_2.[5,6] The dramatic reduction of gate leakage current by five orders of magnitude was achieved by rapid thermal processing (RTP) and deuterium annealing of 2.2 nm SiO_2.[5,6] This improvement was suggested to be caused by strengthening Si–O bonds due to enhanced phonon-energy coupling between Si–O and Si–Si bonds.[6,7] On considering the fact that Si–O and Si–Si bonds exist in HfSiON, it is expected that the RTP and deuterium processing of HfSiON may also improve its gate leakage current. In this letter, we report the leakage current reduction of HfSiON using PECE effect and its scalability down to 5 Å.

The *p*-type Si (100) substrates were cleaned by Radio Corporation of American (RCA) cleaning with $NH_4OH:H_2O_2:H_2O$ and $HCl:H_2O_2:H_2O$ followed by etching in a diluted HF (30:1) solution to remove native oxide and contaminations. The HfSiON films were deposited on the Si wafers by cosputtering (AJA International, ATC 2000 sputtering system) of Hf and Si targets in the presence of Ar, O_2, and N_2 gases.[8] These films were submitted to different RTP sequences in N_2 flow at different temperatures (900–1100 °C) and time intervals (30–60 s). Also, we prepared control samples without any RTP treatments. The physical thicknesses of HfSiON layers were measured using ellipsometry. The compositions of the films were determined using x-ray photoelectron spectroscopy analysis. Al metal gates of 1000 Å thickness were deposited using thermal evaporation system (EDWARDS AUTO 306) through patterns of 7.85×10^{-5} cm^2 made by standard photolithography using SU-8 photoresist. Evaporated aluminum was also used for back side metallization. The final sintering was done at 450 °C in deuterium gas for 30 min. Electrical characterizations of the deposited gate dielectrics were performed using current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements. An Agilent 4155 B semiconductor parameter analyzer was used for *I-V* analysis and Keithley 590 CV for the *C-V* characterizations at 100 kHz and 1 MHz. Equivalent oxide thicknesses (EOTs) for HfSiON films in between 5.2 and 12.3 Å were extracted.

The leakage current characteristics for both control and RTP-annealed HfSiON with EOT of 12.3 Å are shown in Fig. 1. There is a large reduction of leakage current density (one- and-a-half orders of magnitude) for RTP-annealed sample at 1100 °C for 1 min, compared with that of the control sample. Further, it should be noticed that the leakage current also decreases by an order of magnitude for different annealing temperatures varying from 900 to 1100 °C. This

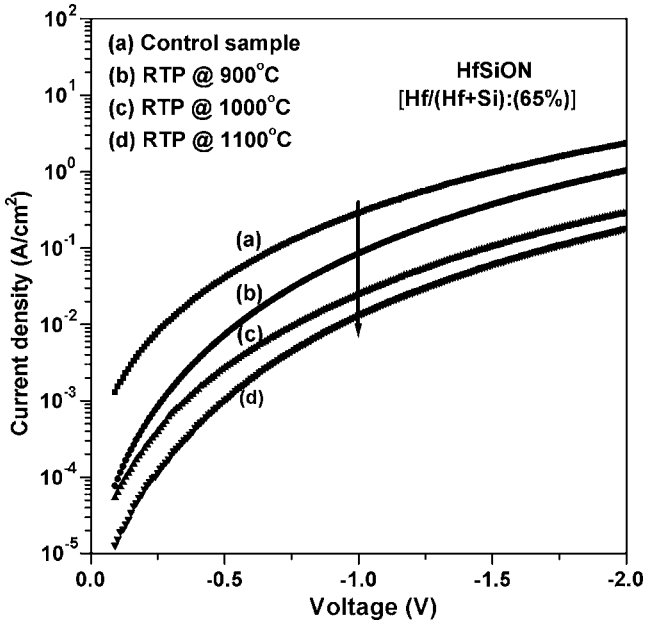

FIG. 1. Gate leakage current density vs gate voltages for control and rapid thermal annealed HfSiON [Hf/(Hf+Si): 65%] samples at different temperatures ranging from 900 to 1100 °C for 1 min in N_2 ambient.

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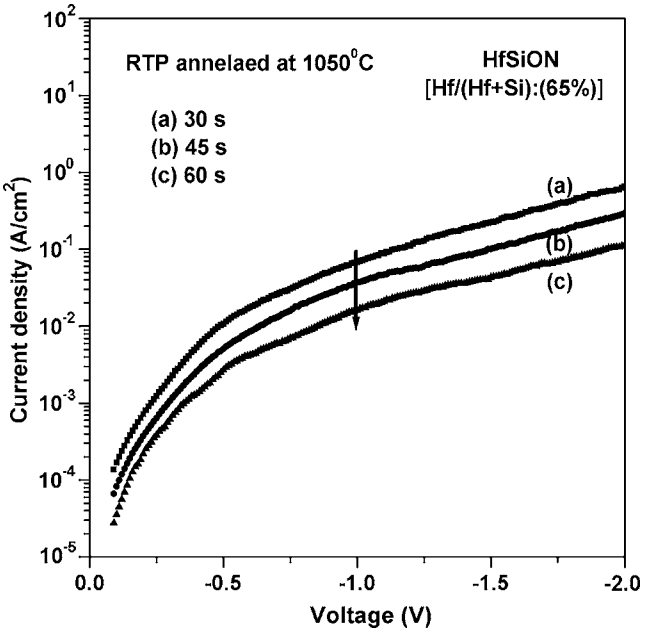

FIG. 2. Variation of leakage with voltage for HfSiON samples for different annealing durations varying from 30 to 60 s in N_2 at 1050 °C.

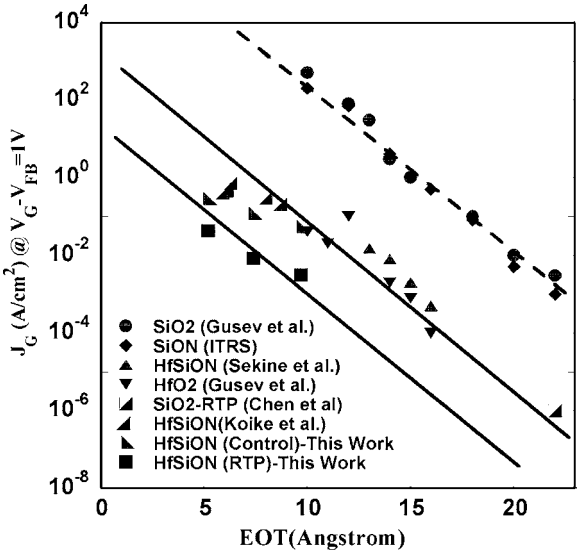

FIG. 3. Current density at a fixed gate bias at $V_G - V_{FB} = -1$ V as function of the equivalent oxide thickness (EOT) for HfSiON/Si. EOT can be scaled down to 5.2 Å, showing improved scalability. Trend lines for SiO_2/SiON [Gusev *et al.* (Ref. 10) and Ref. 13], previous HfSiON data [Sekine *et al.* (Ref. 9), Gusev *et al.* (Ref. 10), and Koike *et al.* (Ref. 8)], and SiO_2 treated by RTP [Chen *et al.* (Refs. 5 and 6)] are also shown.

improvement in leakage current is attributed to the enhanced phonon-energy coupling.[5,6] In our experiments, we measured the physical thickness of HfSiON samples using ellipsometry before and after RTP and found that it remained the same after high temperature RTP processing. Our results of the PECE effect on SiO_2 also showed that there is no thickness change for SiO_2 after RTP.[6] Thus, the leakage current density measured for HfSiON is not due to the increase in film thickness after RTP, but the strengthened Si–O bonds.[6] In addition, the leakage current characteristics of HfSiON with different annealing times were also measured as shown Fig. 2. The leakage current of the sample processed in RTP for 60 s at 1050 °C was 7×10^{-2} A/cm^2 at $V_G - V_{FB} = -1$ V, lower than that processed in RTP for 30 s (4.3×10^{-1} A/cm^2). Therefore, RTP processing for 60 s may enhance the film quality of HfSiON films, probably due to the optimized processing parameters.

The leakage current of the HfSiON films as a function of EOT is shown in Fig. 3. The data show a reduction of leakage current by five orders of magnitude for HfSiON with PECE effect added, comparing to that of untreated silicon oxynitride. The leakage current is also one order smaller than other reported results of HfSiON and HfO_2.[8–10] Koike *et al.* reported the lowest EOT of 6.0 Å estimated for HfSiON [Hf/(Hf+Si):80%], which is applicable to 45 and even 32 nm node high performances Si large scale integrations.[8] We report here a leakage current of 2.8×10^{-1} A/cm^2 at $V_G - V_{FB} = -1$ V for the HfSiON [Hf/(Hf+Si)=50%] with an EOT of 5.2 Å. Its leakage current is further reduced to 4.3×10^{-2} A/cm^2 after RTP and deuterium anneal. We believe that the HfSiON film with higher Si content (~50%) and which undergone high temperature annealing at 1050 °C for 60 s has neither crystallization nor interfacial SiO_2 growth as reported earlier.[11] This is due to the film's amorphous nature and high thermal stability at high temperature in the presence of increased Si content. In addition, in Fig. 3, it should be noted that the pure silicon oxide with the PECE effect added exhibits leakage current reduction similar to that of Hf-based high-k oxides at a larger EOT (2.2 nm).[5,6]

The leakage current of the HfSiON gate dielectric is caused by direct tunneling in our case. It was reported that the leakage current depends not only on the film thickness but also on the effective electron mass and/or barrier height of the film.[12] We might suggest that energy coupling might help increase the electron effective mass and energy band gap of the oxide. One might view that the energy band gap is the energy needed to free valence electrons of Si–O bonds. With the enhanced energy coupling, much large energy is needed to free the valence electrons. Thus the corresponding energy band gap might be increased. This might result in a reduction of direct tunneling current.

In summary, we have investigated the effect of phonon-energy-coupling enhancement effect on the improvement of leakage current for HfSiON films. The leakage current is reduced by one- and-a- half orders of magnitude after RTP and deuterium annealing of HfSiON gate dielectrics. HfSiON, with the help of the PECE effect, can be scaled down to below 5 Å.

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