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Dramatic reduction of gate leakage current of ultrathin oxides through oxide structure modification ☆

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Abstract

We study in detail a new effect, *phonon-energy-coupling enhancement (PECE) effect*, produced by rapid thermal processing (RTP). It includes two aspects: (1) strengthening Si–D bonds and Si–O bonds and (2) change of energy band structure and effective mass. It is shown that not only Si–D bonds but also Si–O bonds have been strengthened dramatically, leading to enhancement of robustness of the oxide structure and the oxide/Si interface. For thick oxides (>3 nm), the gate leakage current has been reduced by two-orders of magnitude and the breakdown voltage has been improved by ~30% due to phonon energy coupling. For ultrathin oxides (2.2 nm), the direct tunnelling current has been reduced by five orders of magnitude, equivalent to that of HfO_2, probably due to increased effective mass and barrier height.

Keywords: Gate oxide; Leakage current; Phonon; Coupling

1. Introduction

In order to pack more devices into a single chip and improve their performance, semiconductor industry has been aggressively scaling MOS devices. As gate oxide is scaled down to below 3 nm, one of the fundamental limitations is the exponential increase in gate leakage current due to quantum tunnelling [1]. High-*k* gate oxides are considered as candidates to replace silicon dioxide or oxynitride [2–4]. However, there are a number of challenging issues facing high-*k* gate oxides, e.g. threshold and flat-band voltage shifts, low mobility, and Fermi-level pining at the metal-gate/oxide interface [2–4]. The most difficult issue for high-*k* gate oxides is the low-*k* interfacial oxide layer, which dominates the dielectric constant. Therefore, this layer makes high-*k* oxide very difficult to be scaled down to less than 0.5 nm. If the leakage current of the oxide or oxynitride can be reduced by several orders of magnitude through the structure modification, the oxide/oxynitride may be further scaled down to the ultimate limit.

In 1996, Lyding et al. [5] discovered the hydrogen/deuterium (H/D) isotope effect of hot-electron degradation of MOS transistors. This discovery has generated widespread interests [6–11]. However, the H/D isotope effect has no effect on improvement of gate oxide [10,11]. The Si–H/D bond-breaking at the SiO_2/Si interface is determined by two competing processes. One is that the energy of the bonds is accumulated through excitation by energetic hot electrons [12,13]. The other process is de-excitation where the bond energy is taken away by coupling [14]. It was suggested theoretically that the isotope effect is originated from the energy coupling from the Si–D bond to

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the Si–Si TO phonon mode, which significantly strengthens the Si–D bonds [14]. Wei et al. [15] confirmed the above theory based on study of vibrational modes of hydrogenated and deuteriated amorphous silicon. In 2000, one of us (Chen) noticed that there is large mismatch between the Si–D vibrational mode (510 cm^{-1}) and the Si–Si TO phonon mode (495 cm^{-1}) based on data of amorphous silicon and proposed a bold hypothesis that if a similar mismatch exists in the SiO_2/Si system and if the Si–D vibrational mode can be shifted toward the Si–Si TO mode, the H/D isotope effect might be dramatically enhanced [16]. In 2003, we confirmed Van de Walle and Jackson's theoretical prediction in the SiO_2/Si system using Fourier transform infrared (FTIR) spectroscopy [17]. There was a new finding that energy is also coupled from Si–D bonds to Si–O bonds (Rocking mode). The mismatch does exist in the SiO_2/Si system as shown in [17], i.e. the Si–D vibrational mode (490 cm^{-1}) does not match the Si–Si TO mode (468 cm^{-1}). In order to accomplish the above proposed objective [16], we attempted to shift the vibrational modes using mechanical and electrical stresses. However, no energy coupling enhancement was observed except for a small shift of the Si–Si TO mode (6–8 cm^{-1}). After numerous trials and failures, we decided to pursue thermal stress.

The ideal thermal stress tool is rapid thermal process (RTP), widely used in semiconductor industry. By directly treating the furnace-grown SiO_2 using RTP at 1050 °C, we discovered the *phonon-energy-coupling enhancement (PECE) effect* of the SiO_2/Si system [18–20]. To our *great surprising*, this effect results in strengthening not only Si–D bonds, leading to further improvement of hot-electron-induced degradation [18], but also Si–O bonds, leading to large reduction of leakage current and improvement of breakdown voltage of SiO_2 [19,20]. Because of limited page space of the previous report and conference abstracts [18–20], it was impossible to have a thorough study of this effect. In this paper, we will study in detail the PECE effect using Fourier Transform Infrared spectroscopy (FTIR) and electrical characterization of MOS transistors and capacitors.

2. Experiment

In our proof-of-concept experiments, we used n^+ silicon wafers ($n = 1 \times 10^{19}$ cm^{-3} and $\rho = 5 \times 10^{-3}$ Ω cm) with (100) orientation, 50 mm (2 inch) in diameter, and ~0.3 mm in thickness. Because high-density electrons are present at the SiO_2/Si interface in MOS transistors, we use n^+ silicon wafers to imitate the situation. The wafers were prepared using conventional RCA cleaning. For thick oxide (>3.5 nm), thermal oxidation was performed in 100% O_2 at 900 °C. For thin oxide (<3.5 nm), thermal oxidation was performed in diluted oxygen (6% O_2) at 900 °C. Because it is unlikely to have the exact same oxide for each wafer, in order to have accurate comparison, the oxidized wafer was cut into two half-wafers. One half-wafer was used as a control sample without further processing and the other half was subjected to rapid thermal processing (Modular Process Technology Co. RTP-600S). The temperature was ramped up to 1050 °C at 27 °C/s, maintained for 1–4 min in N_2, and ramped down at 50 °C/s. Infrared absorbance spectra of the processed wafers were obtained immediately using a Fourier Transform Infrared (FTIR) Spectrometer (Thermo Electron Co., Nexus 470), in conjunction with a variable angle specular reflectance accessory (Pike VeeMax II). The spectral range was selected from 400 to 900 cm^{-1}, with a resolution of 8 cm^{-1}. After this, the RTP processed wafer was annealed in furnace in 100% D_2 or 100% H_2 at 450 °C for 30 min, and then infrared spectra of the sample were obtained again. The MOS capacitors were also fabricated by direct evaporation of 120 nm-thick aluminium layer on top of the oxide using a shadow mask and 100-nm thick Al layer at the back of the exposed n^+-substrate. The MOS capacitors were annealed at 450 °C in 100% D_2 or 100% H_2 for 30 min. (During the manuscript proof reading, we found that the yield of 80% can be obtained if one performs deuterium anneal right after back Al contact deposition and before top Al gate deposition. No anneal should be performed after top Al gate deposition to avoid Al spiking effect.) The oxide thickness was measured using an ellipsometer (Gaertner Scientific Co.). The oxide quality was evaluated by measuring the gate leakage current of MOS capacitors using Agilent 4155B semiconductor analyzer. In order to perform *C–V* measurement, MOS capacitors on p^- Si wafers ($n = 4 \times 10^{15}$ cm^{-3}) were also fabricated using the above processes. High frequency *C–V* curves of MOS capacitors on p-Si wafers were measured using Keithley 590 CV analyzer.

3. Results and discussion

3.1. FTIR study of phonon energy coupling enhancement

Fig. 1 shows vibrational modes of an as-grown SiO_2/Si sample (Curve 1), a SiO_2/Si sample treated in RTP only

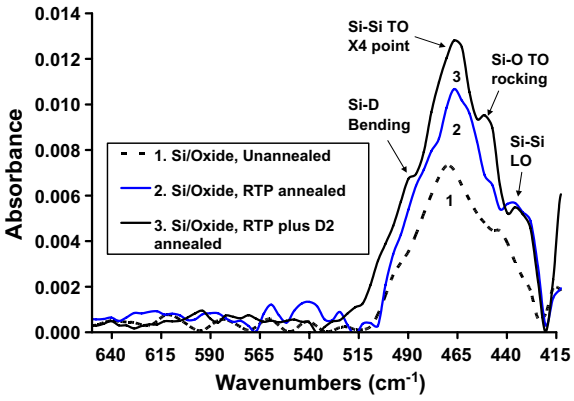

Fig. 1. FTIR spectra of Si/SiO_2 samples (23 nm oxide) based on n^+ wafers ($n = 1 \times 10^{19}$ cm^{-3} and $\rho = 5 \times 10^{-3}$ Ω cm): (1) without any annealing, (2) with RTP annealing (1050 °C in nitrogen for 4 min), and (3) with RTP (1050 °C in nitrogen for 4 min) plus deuterium annealing (450 °C for 30 min).

(Curve 2), and a SiO_2/Si sample treated in RTP plus D_2 anneal (Curve 3). When the SiO_2 is subjected to RTP process only (Curve 2), the Si–Si TO phonon mode, Si–O TO rocking mode, and the Si–Si LO mode are dramatically enhanced. It should be noted that vibrational modes are not shifted after the RTP process on considering the resolution of 8 cm^{-1}. The enhancement for the Si–Si TO mode is about 50%, which is much larger than that for deuterium anneal only (~25% [17]). When the SiO_2 is subjected to RTP plus D_2 anneal, the Si–Si TO phonon mode, Si–O TO rocking mode, and Si–D bending mode are all dramatically enhanced. The enhancement for the Si–Si TO mode is about 73% which is about three times larger than that for deuterium anneal only (~25% [17]).

The phonon-energy-coupling enhancement (PECE) effect might involve several chemical bonds at the interface and also in the bulk of oxide and Si, including Si–D, Si–Si, and Si–O bonds. The deuterium anneal itself results in weak phonon-energy coupling among the Si–D bending mode (490 cm^{-1}), the Si–Si TO mode (468 cm^{-1}), and the Si–O TO rocking mode (448 cm^{-1}) (see Curve 2 and Curve 3 in Reference [17]). The RTP process alone results in larger phonon-energy coupling among the Si–Si TO mode (468 cm^{-1}), the Si–O rocking mode (448 cm^{-1}), and the Si–Si LO mode (435 cm^{-1}) (see Curve 1 and Curve 2 in Fig. 1). The combination of the RTP and deuterium anneal results in the largest energy coupling (see Curve 1 and Curve 3 in Fig. 1). It is well-known in the infrared spectroscopy community that the surface plasmon on the nanoscale metallic islands also produces strong surface-enhanced IR spectra. There is some possibility that RTP might rough the surface of n+ Si so that metallic islands-like structure might occur and thus the observed IR absorption enhancement might be caused by surface plasmon but not by energy coupling. In order to avoid the metallic island-like surface, we used n^- wafer ($n = 2\times10^{14}$ cm^{-3} and $\rho =$ 20.8 Ω cm) for experiments. Fig. 2 shows that the IR absorption enhancement is clearly seen for the n^- silicon wafers, thus it is highly likely that the enhancement is due to energy coupling.

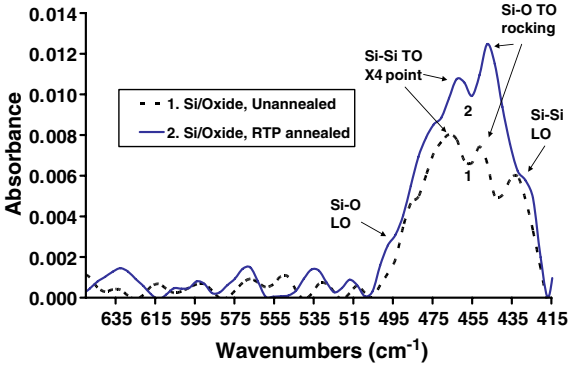

Fig. 2. FTIR spectra of Si/SiO_2 wafers based on n^- wafers ($n = 2\times10^{14}$ cm^{-3} and $\rho = 20.8$ Ω cm): (1) without any annealing and (2) with RTP annealing (1050 °C in nitrogen for 2 min). The oxide thickness is 29 nm.

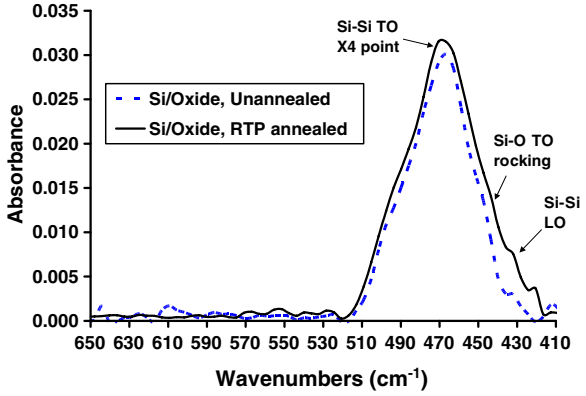

Fig. 3. FTIR spectra of thick-oxide samples (80 nm): Si/SiO_2 samples based on n^+ wafers ($n = 1\times10^{19}$ cm^{-3} and $\rho = 5\times10^{-3}$ Ω cm) without any annealing and with RTP annealing (1050 °C in nitrogen for 4 min).

We suggest that the thermally-induced PECE effect might be caused by change of the oxide microstructure (Stress and bond-angle change) due to thermal effect [21]. The rapid cooling-down (50 °C/s) likely preserve the microstructure change of the oxide, because we did not observe the PECE effect when the SiO_2/Si sample was annealed in furnace for slow ramp-up (0.33 °C/s) and ramp-down (~0.1 °C/s). From Fig. 3, it can be seen that if the oxide is thicker than 800 Å, there is no PECE effect after the RTP process, except for a slight enhancement of the Si–Si LO mode. This thickness dependence suggests that it is a stress-related phenomenon. This also suggests that the PECE effect may not exist for the polysilicon/oxide stack that might have larger tolerance for thermal shock.

Because of the impact of the thermal shock during the RTP process, the more Si–Si TO, Si–O rocking and the Si–Si LO modes might be activated. The activated Si–Si TO modes and Si–O TO modes due to RTP may serve as energy sink for the Si–D bending mode. Therefore, the energy of the Si–D bending mode is more efficiently coupled to other modes after the RTP process, resulting in more robust Si–D bonds. The experimental results showed that the hot-electron degradation of MOS transistors processed in RTP plus D_2 anneal has been improved by 100 times over the devices annealed in D_2 only [18]. More details will be described below. Theoretically, the same argument may also be applied to the Si–O and Si–Si bonds, and thus more robust Si–O and Si–Si bonds may be expected. The direct experimental evidence for strengthening the Si–D and Si–O bonds is shown in the following paragraphs.

3.2. Strengthening Si–D bonds: improvement of hot-electron degradation

In order to have proof-of-concept experiments for energy coupling, we fabricated large-size MOS transistors. The same effect should be available at the scaled MOS devices. The MOS transistors ff following the conventional MOS processes. The thickness of the gate oxide is ~20 nm

with the gate length of 2 μm and the gate width of 150 μm. In addition to the conventional process, the unique process is to do RTP at 1050 °C in N_2 for 2–4 min directly on the gate oxide right after the oxide growth and before deposition of the gate metal. After metallization, the deuterium anneal was carried out at 450 °C for 30 min in 100% D_2. The hot-electron degradation was characterized using Agilent 4155B semiconductor analyzer.

The MOS transistors were stressed at large drain and gate voltages to accelerate their degradation. From Fig. 4, it can be seen that the threshold voltage V_t shift of the transistor processed in RTP plus D_2 anneal is dramatically suppressed. For ~10 mV shift, the transistor processed in RTP plus deuterium anneal lasts 100 times longer than that processed in deuterium only. The transconductance degradation has also been improved as shown in Fig. 5. For ~3% shift, the transistor processed in RTP plus D_2 anneal lasts 100 times longer than that processed in deuterium only.

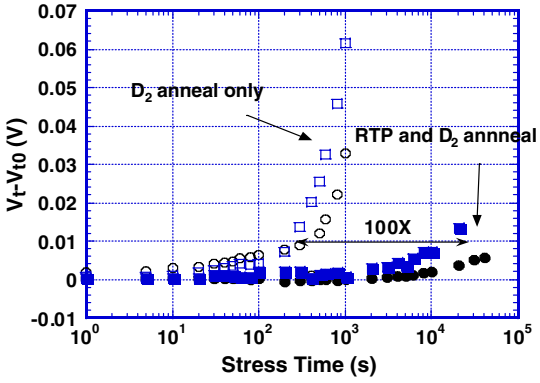

Fig. 4. Comparison of the threshold voltage shift of a MOS transistor processed in deuterium only with that processed in RTP plus deuterium anneal. The devices ($L = 2$ μm, $W = 150$ μm, and $T_{ox} \approx 20$ nm) were stressed at $V_G = 5$ V and $V_D = 12$ V.

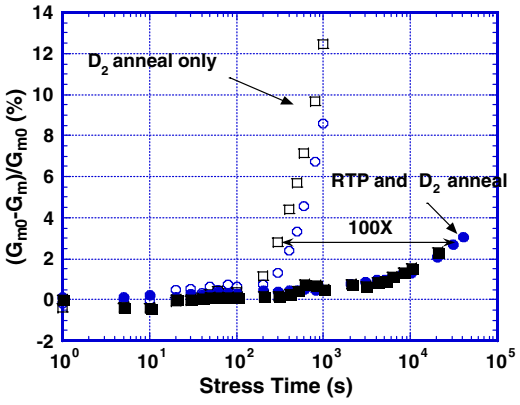

Fig. 5. Comparison of the transconductance degradation of a MOS transistor processed in deuterium only with that processed in RTP plus deuterium anneal. The devices ($L = 2$ μm, $W = 150$ μm, and $T_{ox} \approx 20$ nm) were stressed at $V_G = 5$ V and $V_D = 12$ V.

3.3. Strengthening Si–O bonds: improvement of breakdown and reduction of leakage

Fig. 6 shows schematic of energy coupling from Si–O bonds to Si–Si and Si–D bonds. Fig. 7 shows the effect of H/D isotope effect on the leakage current of silicon dioxide. There is no difference for leakage current between the hydrogen-annealed oxide and the deuterium-annealed oxide. This also confirms previous reports [10,11]. It is interesting to examine the effect of RTP alone on the dielectric strength of oxides. Fig. 8 shows leakage currents of hydrogen-annealed and RTP plus hydrogen-annealed MOS capacitors. Because the vibrational mode of Si–H bonds is far away from the range of 490–448 cm^{-1} [17], there is no energy coupling between the Si–H mode and the Si–Si TO and Si–O rocking modes. Thus, the results shown in Fig. 8 are exclusively from RTP. It can be seen that there is one-order-of-magnitude improvement for leakage current and 10% improvement for the breakdown voltage, resulting from RTP alone. With combination of RTP and deuterium anneal, the leakage current and

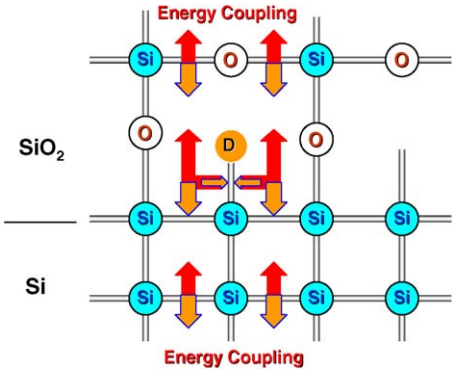

Fig. 6. Schematic illustration of phonon energy from the Si–O rocking mode coupled back to the Si–D bending mode and the Si–Si TO phonon mode.

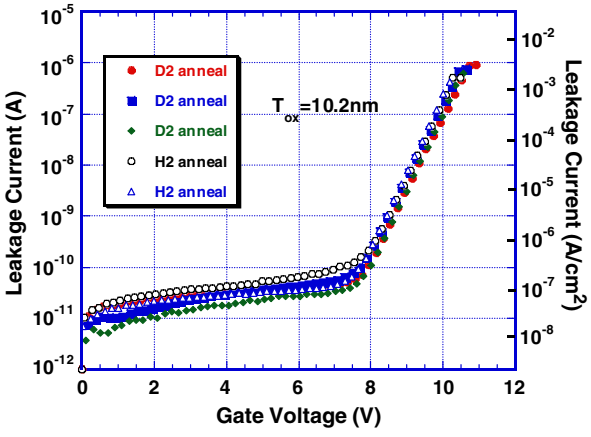

Fig. 7. Gate leakage currents of silicon MOS capacitors with oxide thickness of 10.2 nm and area of 4.24×10^{-4} (cm^2) annealed in hydrogen and deuterium (450 °C for 30 min).

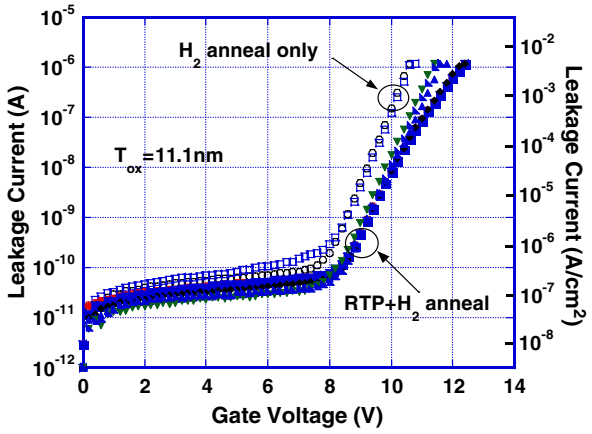

Fig. 8. Gate leakage currents of silicon MOS capacitors with oxide thickness of 11.1 nm and area of 4.24×10^{-4} (cm^2) with hydrogen anneal (450 °C for 30 min) and with RTP (1050 °C in nitrogen for 4 min) plus hydrogen anneal (450 °C for 30 min).

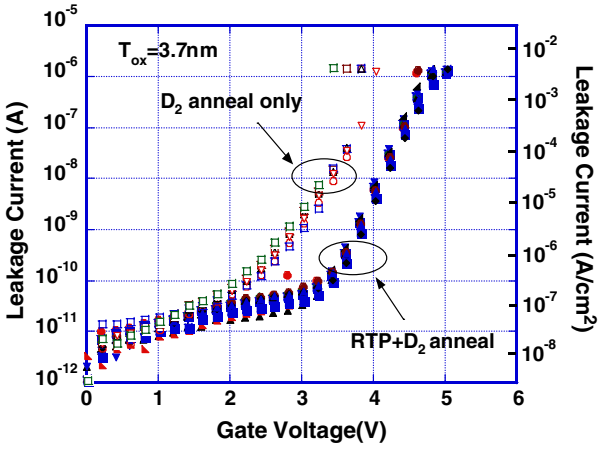

Fig. 10. Gate leakage currents of silicon MOS capacitors with oxide thickness of 3.7 nm and area of 4.24×10^{-4} (cm^2) with D_2 anneal only and with RTP (1050 °C in nitrogen for 4 min) plus deuterium anneal (450 °C for 30 min).

breakdown voltage are further improved as shown in Fig. 9. The leakage current has been improved by two orders of magnitude and the breakdown voltage has been improved by 30%. This result suggests that even if the energy of a single mode, the Si–O rocking mode, was coupled away, the Si–O bonds are significantly strengthened. The above results were obtained from thick oxides (~10 nm). We also fabricated MOS capacitors with thin oxides of 3.7 nm. It can be seen that there are still two-orders-of-magnitude reduction in leakage current and 30% improvement for the breakdown voltage for MOS capacitors processed using RTP plus deuterium anneal (see Fig. 10).

From Figs. 9 and 10, it is clearly seen that the breakdown voltage is increased by 30%. According to the established models [22,23], energetic tunnelling electrons induce defect generation, causing breakdown. With enhanced strength of Si–O bonds, defect generation is reduced, resulting in improved breakdown voltage. Therefore, we expect that the enhanced energy coupling may not only reduce the leakage current but also enhance the reliability of ultra-thin oxides/oxynitrides.

3.4. Reduction of direct tunnelling current

For ultrathin oxide (< 3.5 nm), the dominant leakage current comes from the direct tunnelling. From quantum mechanics theory, the direct tunnelling current may not be affected by the strengthened Si–O bonds. However, to our great surprise, the oxide leakage current for a 2.2 nm-thick oxide is reduced by five orders of magnitude after RTP anneal for 1 min plus D_2 anneal (see Fig. 11). According to a theory proposed by Khairurrijal et al. [24] and refined by Stadele et al. [25], the electron effective mass in the oxide layer tends to increase as the oxide thickness decreases to less than 2.8 nm due to the existence of compressive stress in the oxide layer near the oxide/Si interface. Based on their theory, we may suggest that the increase in

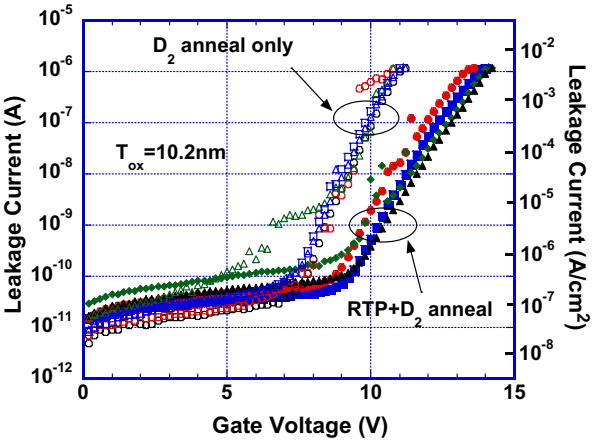

Fig. 9. Gate leakage currents of silicon MOS capacitors with oxide thickness of 10.2 nm and area of 4.24×10^{-4} (cm^2) with D_2 anneal only and with RTP (1050 °C in nitrogen for 4 min) plus deuterium anneal (450 °C for 30 min).

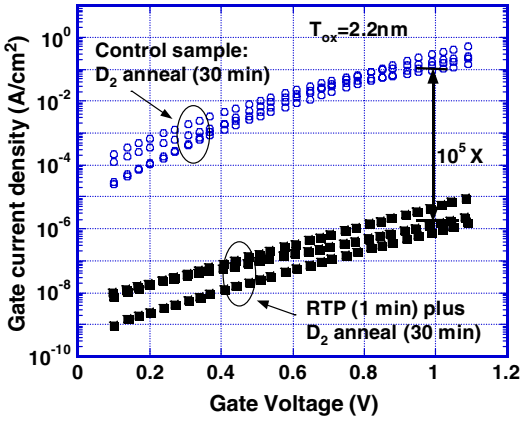

Fig. 11. Gate leakage current density of silicon MOS capacitors with oxide thickness of 2.2 nm on n^+ wafers ($n = 1 \times 10^{19}$ cm^{-3}) with deuterium anneal only (450 °C for 30 min) and with RTP (1050 °C in nitrogen for 1.0 min) plus deuterium anneal (450 °C for 30 min).

electron effective mass due to RTP-induced compress stress may reduce the leakage current. In addition, by fitting our J–V curves to the Simmons' tunnel current theory [26], we find that after RTP the conduction-band barrier height between the oxide (2.2 nm) and Si is increased from 3.0 eV to 4.1 eV and the electron effective mass is slightly increased from 0.3 m_0 to 0.37 m_0 (The detail will be published elsewhere). Therefore, increase in both the effective mass and barrier height after RTP might lead to dramatic reduction of leakage current.

3.5. Factors affecting experimental results

It is of critical importance to examine whether the dramatic leakage current reduction is due to new physics or just thickened oxides due to RTP. Every time, the RTP chamber was flushed thoroughly using N_2 before processing and the oxide thickness was measured using an ellipsometer (Gaertner Scientific) before and after RTP. We did not observe any thickness change of oxides ranging from 1.7 to 80 nm after RTP. Table 1 shows the results of oxide thickness measured before and after RTP for ultrathin oxides. Capacitance–voltage (C–V) measurement was also carried out to clarify this issue. MOS capacitors based on p^- substrates (4×10^{15} cm^{-3}) were fabricated. Fig. 12 shows high frequency capacitance–voltage (C–V) curves for MOS capacitors with oxide of 3 nm before and after RTP. It is very hard to obtain quasi-static C–V curves for oxides thinner than 5 nm. It can be seen that the capacitance in accumulation was not changed after RTP, suggesting that the oxide thickness remains the same after RTP, which is in agreement with our measurements using ellipsometry. There is only a slight flatband-voltage shift after RTP (<0.2 V). Therefore, it is clear that the leakage current reduction is due to the new phenomena. Fig. 13 shows the quasi-static and high frequency curves of an oxide sample with a thickness of 7 nm. Excellent C–V curves suggest that excellent interface properties are maintained after RTP.

Table 1
Comparison of oxide thickness measured before and after RTP

Sample no.	Oxidation parameters	T_{ox} before RTP (Å)	T_{ox} after RTP (Å)
#1110051	N_2 @1000 sccm, O_2 @20 sccm, 900 °C for 20 s	22.4	23.3
#0628052	N_2@1000 sccm, O_2 @20 sccm, 900 °C for 10 s	19.8	20.9
#1110052	N_2 @2000 sccm, O_2 @20 sccm, 900 °C for 20 s	19.5	20.09

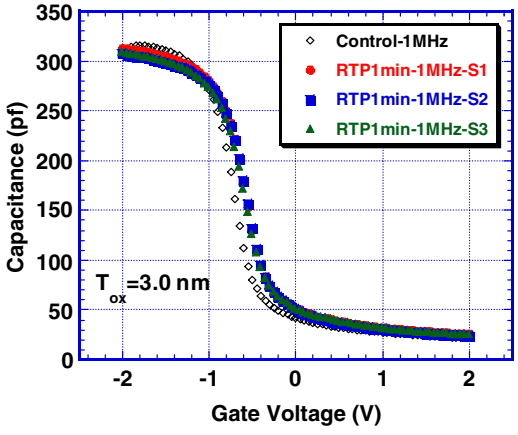

Fig. 12. High-frequency C–V curves of a control sample (before RTP) and samples after RTP at 1050 °C in nitrogen for 1 min with oxide thickness of 3 nm on p-Si (4×10^{15} cm^{-3}). The samples were finally annealed in 100% D_2 at 450 °C for 30 min.

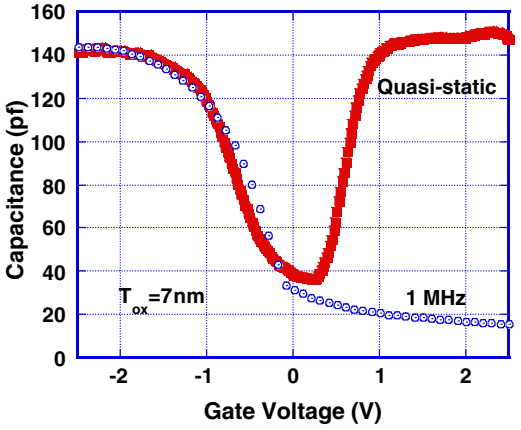

Fig. 13. High-frequency and quasi-static C–V curves of the RTP sample (1050 °C in nitrogen for 1.0 min) with oxide thickness of 7 nm on p-Si (4×10^{15} cm^{-3}). The sample was finally annealed in 100% D_2 at 450 °C for 30 min.

There are several puzzling phenomena that need to be clarified. The industry has been doing RTP for over 20 years. Why didn't the industry find the PECE effect? This effect is very sensitive to processes and process parameters. For example, it is dependent on thickness (see Fig. 3), process temperature, process time-duration, and cooling rates. Some processes actually completely eliminate this effect. Using FTIR as a tool, we were able to exam various process steps. Based on our FTIR studies, we observed the following facts (the details will be published elsewhere). The effect is weakened when the RTP temperature is less than 900 °C. The RTP process time should be reduced as oxide thickness decreases. Our FTIR results also showed that IR enhancement disappeared when the RTP processed sample was exposed to plasma and reduced to half once it was immersed into the developer for regular photoresist (PR). Therefore, the key is to avoid exposure to plasma and the developer for regular PR. Therefore, it is unlikely that the PECE effect can be preserved after various plasma processes in industry. Our results in Fig. 11 (5 orders of leakage current reduction) was obtained from MOS capacitors fabricated by thermal evaporation of Al directly on oxides using a shadow mask without exposure to any chemical and waters. We also found that a PR with neutral developer, e.g. SU8, almost has no damage to this effect.

Although our finding was exclusively originated from our fundamental study of energy coupling of chemical bonds, later we also noticed that the inconsistent results were reported for rapid thermal oxidation (RTO) and rapid thermal nitridation (RTN). One group reported leakage current reduction (3 orders reduction) for RTP- or RTO grown oxynitrides [27] and majority of groups reported no reduction [28–31]. It is found that the one claiming large leakage current reduction [27] accidentally avoid the plasma process by using thermal evaporation of Al gate metal for MOS capacitors so that the PECE effect was preserved. However, the same group [27] also reported gate leakage current of NMOS transistors, which did not show any gate leakage current reduction (Fig. 7 of Ref. 27). This suggests that the PECE effect was lost in the followed plasma processes such as sputtering and dry etching processes during their transistor fabrication. Majority of people claiming no leakage current reduction actually used either too low temperature (800–850 °C) or too short time (10–20 s) in their RTO or RTN growth [28–30]. Therefore, the semiconductor industry did not find this effect simply because either it was lost in the followed plasma processes [27,31] or non-optimized RTP processes [28–30]. More processing experiments are needed to study how to preserve this effect. Further research is needed to understand fundamentally what causes the enhanced energy coupling. Fundamental understanding might lead to further improvement.

4. Conclusions

We studied a new effect for the SiO_2/Si system, *PECE effect*. It includes two aspects: (1) strengthening Si–D bonds and Si–O bonds and (2) change of energy band structure and effective mass. The vibrational modes of the Si–Si and Si–O bonds exhibit enhanced energy coupling when the rapid thermal processing (RTP) is directly applied to the SiO_2/Si system. With combination of the RTP and deuterium (D) anneal, the strongest coupling among the Si–D, Si–Si, and Si–O bonds was observed. It is shown that not only Si–D bonds but also Si–O bonds have been strengthened dramatically, leading to enhancement of robustness of the oxide structure and the oxide/Si interface. The gate leakage current has been reduced by two-orders of magnitude and the breakdown voltage has been improved by ~30% for thick oxides (>3 nm) due to phonon energy coupling. The direct tunnelling current has been reduced by five-orders of magnitude, equivalent to that of HfO_2, probably due to increased barrier height and effective mass. This effect may fundamentally impact the scaling and reliability of modern Si MOS technology.

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