On the Mechanism for Interface Trap Generation in MOS Transistors Due to Channel Hot Carrier Stressing

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Abstract—The classical concept and theory suggest that the degradation of MOS transistors is caused by interface trap generation resulting from "hot carrier injection." We report three new experiments that use the deuterium isotope effect to probe the mechanism for interface trap generation in n-MOS transistors in the presence of hot hole and electron injection. These experiments show clearly that hot carrier injection into the gate oxide exhibits essentially no isotope effect, whereas channel hot electrons at the interface exhibit a large isotope effect. This leads to the conclusion that channel hot electrons, not carriers injected into the gate oxide, are primarily responsible for interface trap generation for standard hot carrier stressing.

Index Terms—CMOS, deuterium, hot-carrier, reliability.

ANY experiments on interface trap generation have been carried out by intentionally injecting hot holes and electrons into SiO₂ [1], [2] and by channel hot carrier stressing or drain avalanche stressing [3]–[7]. (Drain avalanche stressing is a standard hot carrier stressing technique that uses high drain voltage and reasonable gate voltage to produce the maximum substrate current.) More evidence has been provided that the degradation is associated with interface trap creation [5] and oxide trap formation in the vicinity of the drain junction [6]. It is commonly accepted that the interface trap generation is caused by hole and electron injection into the oxide during channel hot carrier stressing or drain avalanche stressing. The recent discovery of the giant deuterium isotope effect in transistor degradation [8]-[11] presents new experimental opportunities for elucidating the underlying degradation mechanism. It is therefore interesting to investigate the deuterium isotope effect for various carrier injection modes into the gate oxide. If the

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widely accepted model of interface trap generation by hot carrier injection is true, then carrier injection experiments should exhibit the same giant isotope effect as has been observed for drain avalanche stressing. Such experiments and their consequences for the mechanism of trap generation are the subject of this letter.

We have performed three experiments to intentionally inject holes and electrons deep into the oxide and also have them present only at the interface. In the experiments, 0.35-µm 3.3-V NMOS transistors with a gate oxide of 65 Å were used. In the first experiment, hot holes were injected into the oxide by applying a negative gate voltage ($V_G = -9 \text{ V}$). A detailed description of hole injection and trapping in the oxide can be found in [12]. For the hole injection experiment, the source, drain, and bulk (p-well) were grounded, and a negative bias (-9 V) was applied to the gate in the dark. In the second experiment, hot electrons were injected deep into the oxide from the substrate. To achieve this, the drain and source were floated, the gate was grounded, and a negative bias from -12 to -17 V was applied to the bulk. The third experiment was designed to direct hot electrons only toward the interface from the substrate. In this experiment, the source and drain were grounded, 1 V was applied to gate, and -11 V was applied to the substrate. A large number of hot electrons (in milliamperes) can be generated by impact ionization in the depletion region. These hot electrons are confined to the immediate region of the interface because of the low gate voltage. In addition, we performed standard drain avalanche hot carrier stressing of NMOS transistors by stressing at the maximum substrate current with $V_D = 5.5 \text{ V}$. The degradation tests were carried out using an HP4155A semiconductor parameter analyzer. The test code was modified to monitor the polarity of the shift of the threshold voltage V_T and the transconductance G_m . The interface traps were monitored by charge-pumping measurements. The set-up consists of the HP4155A, an HP E5250A switching matrix, and a Racal-Dana 2021 programmable pulse generator.

Fig. 1 shows the results from the first experiment, which measures the deuterium isotope effect for the hot hole injection only. The figure shows the time-dependent V_T shift and the interface trap increment for NMOS transistors stressed in the dark at $V_D = V_S = V_B = 0$ and $V_G = -9$ V. Chips from neighboring locations on the same wafer were annealed at 450 °C for 3 h in 100% H₂ and 100% D₂, respectively. It is seen that initially, the threshold voltage shift $(V_T - V_{T0})$ changes toward the negative side, indicating that holes are indeed being injected and trapped

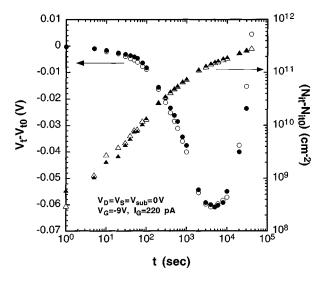


Fig. 1. Time dependence of threshold voltage shift and the interface trap increment for n-MOS transistors annealed at 450 °C for 3 hr. in 100% H₂ (O Δ) and 100% D₂ ($\bullet \blacktriangle$). The devices were stressed at $V_D=V_S=V_B=0$ V and $V_G=-9$ V in the dark.

in the oxide. For absolute values of V_G below 8 V, no significant hole trapping can be observed. After ~3000 s, (V_T-V_{T0}) begins to change toward the positive side, indicating that negative charge starts to build up due to electron injection from the gate. A gate current of ~200 pA was measured. Under these conditions, the interface traps are generated by hole injection. It is quite interesting to note, from Fig. 1, that the isotope effect for hole injection is very small. Over the entire stressing time interval, there is essentially no difference between hydrogen and deuterium annealed devices. Even during the electron injection stage, no isotope effect is observed. This experiment has been repeated several times with the same result.

Fig. 2 shows the results from the second experiment in which hot electrons were injected into the gate oxide with the source and drain floating. The voltages applied across the gate and the substrate were 12 and 17 V, respectively. It is observed that hot electrons, which are deeply injected into the gate oxide, indeed generate interface traps. For $V_G = 0$ V and $V_B = -12$ V, the gate current I_G is 1.8 nA and for $V_G=0~\mathrm{V}$ and $V_B=-17~\mathrm{V}$, the gate current I_G is 15 nA. For $V_G=0~\mathrm{V}$ and $V_B=-17$ V, the initial shift in the first second is very large. After the initial period, the generation rate decreases significantly. The slope for the interface trap generation is even smaller than that for $V_B = -12$ V. This indicates that hot electron injection is not a very efficient process for interface trap generation as has been known before. Again, comparing the deuterium and hydrogen processed devices shows no discernible difference for interface trap generation. This means that there is no isotope effect in this case either.

From the above two experiments, it can be concluded that hole and electron injection into the oxide are not associated with a significant isotope effect in threshold shift and trap generation. The atomic mechanism for the trap generation due to hot carrier injection into the oxide may be related to oxygen vacancies, but has not yet been uniquely determined.

Fig. 3 shows the third experiment where hot electrons are injected only at the interface. In this experiment, the source and

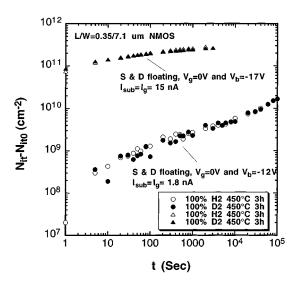


Fig. 2. Time dependence of the interface trap increment for n-MOS transistors annealed at 450 °C for 3 h in 100% H₂ (O Δ) and 100% D₂ (• \blacktriangle). The devices were stressed at $V_G=0$ V and $V_B=-12$ V in the dark with source and drain floated, and at $V_G=0$ V and $V_B=-17$ V in the dark with source and drain floated.

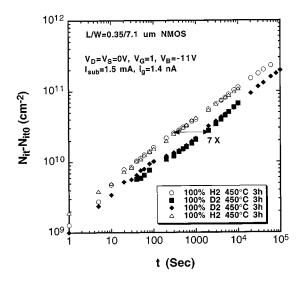


Fig. 3. Time dependence of the interface trap increment for n-MOS transistors annealed at 450 °C for 3 h in 100% H₂ (O Δ) and 100% D₂ (• \blacktriangle). The devices were stressed at $V_D=V_S=0$ V, $V_G=1$ V and $V_B=-11$ V in the dark.

drain were grounded, 1 V was applied to the gate, and –11 V was applied to the substrate. The high-energy electrons produced in the depletion region due to the impact ionization are present just at the interface because of the low gate voltage. After measuring the gate current, the substrate current, the source current, and the drain current, it is found that a large number of hot electrons (~1 mA) are present at the interface and pass through the source and drain. A small amount of gate current (1.4 nA), equivalent to that in the second experiment, was also measured. The key difference, however, is the presence of a high density of channel hot electrons that can interact with the interface without being injected into the oxide. It is found that many more interface traps are generated than in the second experiment, presumably as a result of this interaction. In addition, a notable difference appears in this experiment: the degradation is associated with a large

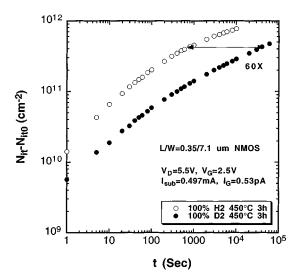


Fig. 4. Time dependence of the interface trap increment for n-MOS transistors annealed at 450 °C for 3 h in 100% H₂ (O) and 100% D₂ (\bullet). The devices were stressed at $V_D=5.5$ V, $V_S=0$ V, $V_G=2.5$ V and $V_B=0$ V in the dark.

isotope effect (7 times). This means that a significant amount of interface traps are generated via a mechanism associated with the isotope effect, i.e., involving hydrogen. This mechanism is very different from that of electron injection into the oxide.

Fig. 4 shows the standard hot carrier stressing (drain avalanche stressing). The n-MOS transistors were stressed at $V_D=5.5~\rm V$, $V_G=2.5~\rm V$, and $V_B=V_S=0~\rm V$. In this case, a giant isotope effect (60 times) is observed. The gate current is very small (only 0.53 pA) for $V_G=2.5~\rm V$, and even when the gate voltage reaches 5.5 V, the gate current is only 70 pA. This indicates that carrier injection is very small. The substrate current and drain current are very large. All of these results indicate that a large amount of interface traps are generated by a mechanism, which is different from that of electron and hole injection into the oxide. Therefore, for standard channel hot carrier stressing, channel hot electrons that are not injected into the gate oxide generate a significant amount of interface traps.

In summary, three new experiments for the deuterium isotope effect for hot hole and electron injection have been performed to probe the mechanism of interface trap generation during normal hot carrier stress. It has been found that hot carrier injection into

the gate oxide is not involved in the deuterium isotope effect. Only hot electron damage at the interface shows the isotope effect. In the standard hot carrier stressing, channel hot electrons, which are not injected into the oxide, generate a significant amount of interface damage. We believe that this modified picture provides a better understanding than the traditionally accepted concept that interface traps are generated mostly by hot hole and electron injection into the oxide.

REFERENCES

- S. K. Lei, "Interface trap generation in silicon dioxide when electrons are captured by trapped holes," *J. Appl. Phys.*, vol. 54, pp. 2540–2546, 1983
- [2] T. H. Ning, C. M. Osburn, and H. N. Yu, "Emission probability of hot electrons from silicon into silicon dioxide," *J. Appl. Phys.*, vol. 48, pp. 286–293, 1977.
- [3] E. Takeda, C. Y. Yang, and A. Miura-Hamada, Hot-Carrier Effects in MOS Devices. San Diego, CA: Academic, 1995.
- [4] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, pp. 2194–2209, 1998
- [5] C. Hu, S. C. Tam, F. C. Hsu, P.-K. Ko, T. Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation-model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 375–385, 1985.
- [6] B. S. Doyle, M. Bourcerie, J.-C. Marchetaux, and A. Boudou, "Interface trap creation and charge trapping in the medium-to-high gate voltage range $(V_d/2 \le V_g \le V_d)$ during hot carrier stressing of n-MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 744–754, 1990.
- [7] B. S. Doyle, M. Bourcerie, C. Bergonzoni, R. Benecchi, A. Bravis, K. R. Mistry, and A. Boudou, "The generation and characterization of electron and hole traps created by hole injection during low gate voltage hot-carrier stressing of n- MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 1869–1876, 1990.
- [8] J. W. Lyding, K. Hess, and I. C. Kizilyalli, "Reduction of hot electron degradation in MOS transistors by deuterium processing," *Appl. Phys. Lett.*, vol. 68, pp. 2526–2528, 1996.
- [9] I. C. Kizilyalli, J. W. Lyding, and K. Hess, "Deuterium post-metal annealing of MOSFET's for improved hot carrier reliability," *IEEE Elec*tron Device Lett., vol. 18, pp. 81–83, 1997.
- [10] K. Hess, I. C. Kizilyalli, and J. W. Lyding, "Giant isotope effect in hot electron degradation of metal oxide silicon devices," *IEEE Trans. Elec*tron Devices, vol. 45, pp. 406–416, 1998.
- [11] R. A. B. Devine, J.-L. Autran, W.-L. Warren, K. L. Vanheusdan, and J.-C. Rostaing, "Interfacial hardness enhancement in deuterium annealed 0.25 µm channel metal oxide semiconductor transistors," *Appl. Phys. Lett.*, vol. 70, pp. 2999–3001, 1997.
- [12] K. F. Schuegraf and C. Hu, "Hole injection SiO₂ breakdown model for very low lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, pp. 761–767, 1994.