using zero $V_D$ in extracting asymptotic $V_T$ is minimal. A final note is that $V_T$ extracted in this paper is intended for the threshold voltage of strong inversion, and a different $V_T$ may be needed for characterizing the onset of subthreshold region.

## V. Conclusions

Design and modeling of submicron MOSFETs require an accurate theoretical definition for the threshold voltage $V_T$. A new approach for defining $V_T$ has been proposed based on the intersection of the surface potential asymptotes for the depletion and strong inversion regions. It was shown that the threshold voltage defined by such an approach offers a better agreement with $V_T$ extracted from the drain-current versus gate-voltage characteristics than those predicted by the conventional and other modified definitions. In particular, it was demonstrated in the device simulation environment that the new approach provides a greater accuracy than other existing definitions for both long- and short-channel MOSFETs having various oxide thicknesses and substrate doping densities.

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# Deuterium Isotope Effect for AC and DC Hot-Carrier Degradation of MOS Transistors: A Comparison Study

Zhi Chen, Kangguo Cheng, Jinju Lee, Joseph W. Lyding, Karl Hess, and Sundar Chetlur

***Abstract*—Several new phenomena are observed comparing the ac stress with the dc stress. In the initial stress period ($<$ 30 s), the deuterium isotope effect is smaller for ac stress than for dc stress, which is ascribed to the hole injection. In the final stress stage ($>$ $10^4$ s), the saturation of the $G_m$ degradation stops and the $G_m$ degradation starts to increase again for ac stress, which is probably due to the hole trapping.**

***Index Terms*—CMOS, deuterium, hot-carrier, reliability.**

## I. Introduction

The discovery of the giant deuterium isotope effect in hot-carrier degradation of MOS transistors has fueled the industrial development of the use of this effect to improve the reliability of integrated circuits [1]–[8]. On the other hand, the deuterium isotope effect can be used as an effective tool to help solve the long-standing mystery of hot-carrier degradation mechanisms in MOS transistors [9]–[11]. Some researchers suggested that the degradation is caused by both hole and electron injection into the oxide [12]–[14]. Recently, we showed direct experimental evidence to support the new theory that the dominant degradation mechanism is the direct interaction of hot electrons with Si–H/D bonds [9]–[11]. All of the above hot-carrier degradation experiments are carried out in dc stress. However, MOS transistors in real integrated circuits work in an ac dynamic environment. It is very important to study the deuterium isotope effect for devices under ac stress. In addition, the role of holes in the isotope effect is not very clear. In order to collect more evidence, we study the ac stress with the gate pulsed from 0 to 3 V, because more holes are injected in this bias. In this brief, we report for the first time, the study of the deuterium isotope effect in ac hot-carrier degradation.

In the experiments, 0.35-$\mu$m 3.3 V n-MOS transistors with a gate oxide of 65 Å were used. The devices consist of phosphorus-implanted LDD source and drain, oxide spacers, and three levels of metallization. The devices were annealed in 100% $H_2$ or 100% $D_2$ in conventional furnace (one atmosphere) for 3 h. During the ac stress, the drain was connected to a constant voltage of 5.5 V, while the gate was pulsed between 0 V and 3 V with a pulse period of 2 $\mu$s, a pulsewidth of 1 $\mu$s, and both the rise and fall times of 100 ns. In order to compare the ac stress with the dc stress, the dc stress was carried out in similar devices and duty cycles of the ac stress were considered. For the dc stress, the transistors are stressed at $V_D = 5.5$ V and $V_G = 3$ V (maximum $I_{\rm sub}$). In order to assure that holes are injected into the oxide region above the channel outside the drain, $V_D$ should be larger than the critical drain voltage $V_D^*$ [14]. In our case, the critical drain voltage $V_D^*$ was found to be 5.2 V. We found that under the condition of $V_D = 5.5$ V and $V_G = 0.6$ V, the maximum hole injection was produced. Therefore, we chose $V_D = 5.5$ V for the ac and dc stress. The degradation tests

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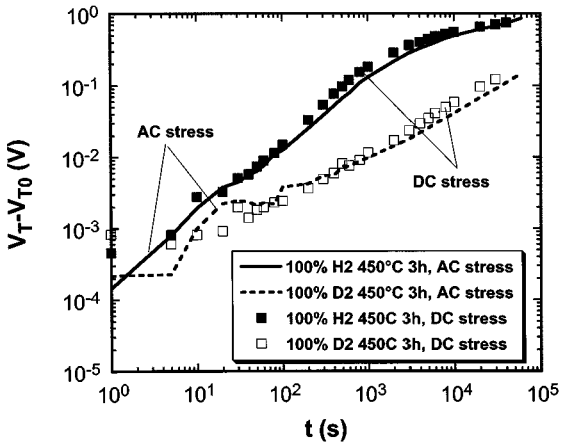


Fig. 1. Time dependence of threshold voltage shift for n-MOS transistors annealed at 450 °C for 3 h in 100% $H_2$ and 100% $D_2$ under ac stress and dc stress. The devices were stressed in ac at $V_D = 5.5$ V, $V_S = 0$ V, and $V_G(\text{pulse}) = 0$–3 V with a 2-$\mu$s period and a 1-$\mu$s pulsewidth in the dark and were stressed in dc at $V_D = 5.5$ V, $V_S = 0$ V, and $V_G = 3$ V in dark.

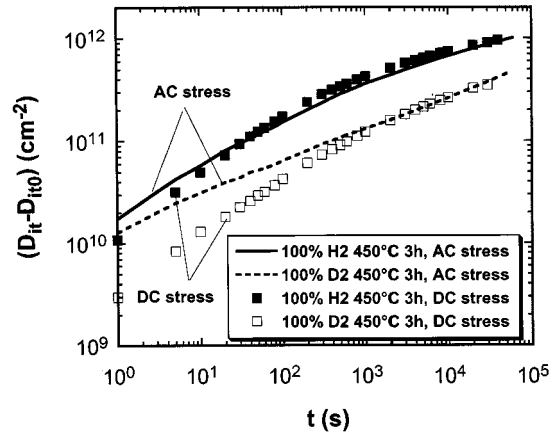


Fig. 3. Time dependence of the interface trap increment for n-MOS transistors annealed at 450 °C for 3 h in 100% $H_2$ and 100% $D_2$ under ac stress and dc stress. The devices were stressed at $V_D = 5.5$ V, $V_S = 0$ V, and $V_G(\text{pulse}) = 0$–3 V with a 2-$\mu$s period and a 1-$\mu$s pulsewidth in the dark and were stressed in dc at $V_D = 5.5$ V, $V_S = 0$ V, and $V_G = 3$ V in dark.

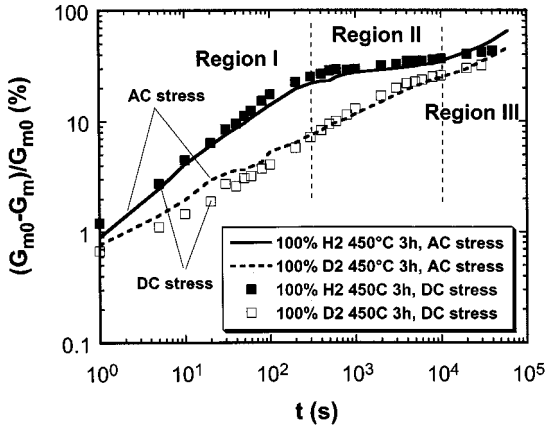


Fig. 2. Time dependence of the transconductance degradation for n-MOS transistors annealed at 450 °C for 3 h in 100% $H_2$ and 100% $D_2$ under ac stress and dc stress. The devices were stressed at $V_D = 5.5$ V;$V_S = 0$ V, and $V_G(\text{pulse}) = 0$–3 V with a 2-$\mu$s period and a 1-$\mu$s pulsewidth in the dark and were stressed in dc at $V_D = 5.5$ V, $V_S = 0$ V, and $V_G = 3$ V in dark.

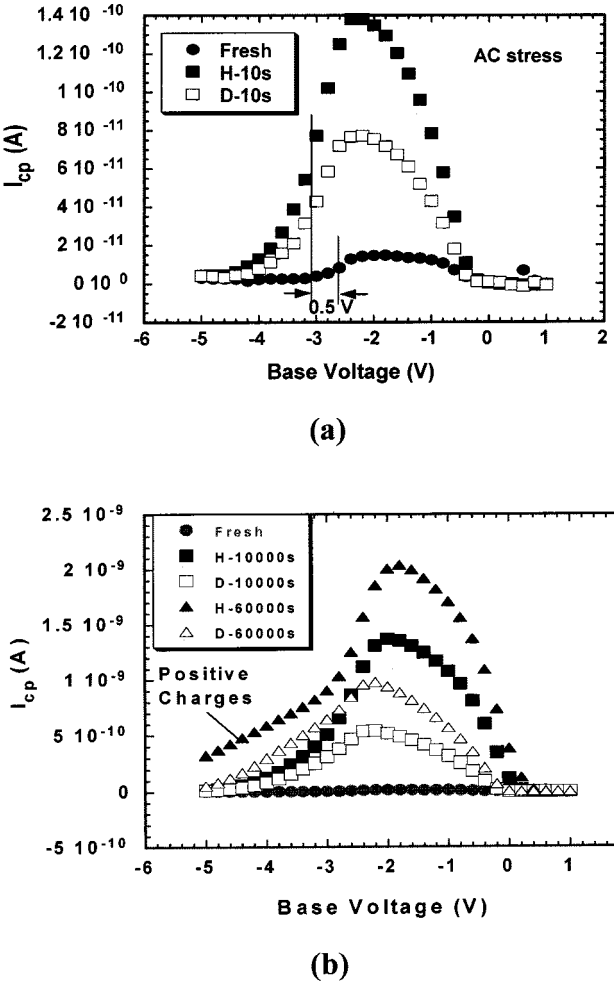


Fig. 4. CP curves for n-MOS transistors annealed at 450 °C for 3 h in 100% $H_2$ (solid symbols) and 100% $D_2$ (open symbols) under ac stress for (a) 10 s and (b) 60 000 s. The devices were stressed at $V_D = 5.5$ V, $V_S = 0$ V, and $V_G(\text{pulse}) = 0$–3 V with a 2-$\mu$s period and a 1-$\mu$s pulsewidth in the dark. The CP current shift is defined as the shift at the half of the peak between the fresh and the stressed devices processed in deuterium.

were carried out using an HP4155A semiconductor parameter analyzer. The interface traps were monitored by charge-pumping (CP) measurements. The setup consists of an HP4155A, an HP E5250A switching matrix, and a Racal–Dana 2021 programmable pulse generator. The maximum $G_m$ was measured at $V_D = 0.1$ V and $V_T$ is defined at $I_D = 1$ $\mu$A*W/L. The resolution for the voltage measurement is 20 $\mu$V.

Figs. 1–3 show the $V_T$ shift, $G_m$ degradation, and interface trap generation for both ac and dc stress. The giant isotope effect is observed in all of the above three figures, indicating that the deuterium anneal helps improving the reliability of the actual operating integrated circuits. It is also seen that the isotope effect for ac stress is smaller in the initial stage in all three figures than it is for dc stress. This is due to the hole trapping in the initial stage because in our ac stress arrangement, holes favor to be trapped in the oxide outside the drain. It was shown previously that the interface traps created by trapped holes did not exhibit the isotope effect [9]–[11]. Therefore, for ac stress, in the initial stage, less isotope effect should be observed. For dc stress, because $V_G$ is fixed at 3 V and $V_D$ is set at 5.5 V, holes do not favor to be trapped in oxide. Therefore, for dc stress, larger isotope effects exhibit in the initial stage, as shown in Figs. 1–3. Fig. 4(a) shows the CP current for the same n-MOS transistors stressed for 10 s in ac stress. The CP curve for the deuterium-processed device shifts toward the left-hand side (LHS) by 0.5 V in ac stress, while the curve only shift 0.2 V in dc stress (not

shown here). Partially, this shift may be due to the positive charge [15]. Although the nonuniformity of the damage also causes curves shifting toward the LHS the magnitude of the shift in ac stress is too large to be considered solely as the nonuniformity [15].

The most intriguing phenomena are observed in the $G_m$ degradation as shown in Fig. 2. In Region I, the $G_m$ degradation increases rapidly. However, in Region II, the $G_m$ degradation begins to be saturated. This does not mean that generation of interface traps stops, because Fig. 3 shows clearly the continuous generation of interface traps in Region II. The $G_m$ saturation is caused by less scattering from the interface traps because the negative charges built up by the acceptor-type interface traps repel the channel electrons away from the interface. It looks that there is no saturation for the deuterium-processed transistor (dotted line). However, if one takes a close look at the plot in Fig. 2, one can find a slight saturation at $\sim 8 \times 10^3$ s for the D-processed sample. It is very surprising that for ac stress, at around $10^4$ s, the $G_m$ degradation starts to increase again (Region III). On the other hand, the $G_m$ degradation does not increase in Region III for dc stress. In order to understand the phenomena better in Region III, the CP currents for transistors stressed in ac for $10^4$ s and $6 \times 10^4$ s are presented in Fig. 4(b). Because the results from the $10^4$ s-point still represent Region II and those from $6 \times 10^4$ s-point represent Region III, these results should reveal what happens in these two regions. It is interesting to see that the CP current tails appear at the LHS at $6 \times 10^4$ s under ac stress, which should be due to the positive charges [14]. This unique tail is the cause for the increase in the $G_m$ degradation during ac stress in Region III, because at $10^4$ s, there is no such a tail. There is no such a tail either in CP current for the H-processed transistor at $6 \times 10^4$ s for dc stress (not shown here). This is in agreement with the fact, as shown in Fig. 2, that there is less increase in $G_m$ degradation in Region III for dc stress. The above evidence strongly supports that this unique tail is the cause for the $G_m$ degradation increment for devices stressed for over $10^4$ s. These positive charges which should be trapped holes may attract the channel electrons back toward the interface. This may increase the interface scattering, causing the increase in the $G_m$ degradation.

In summary, several new phenomena are observed comparing the ac stress with the dc stress. In the initial stress period ($<30$ s), the deuterium isotope effect is smaller for ac stress than for dc stress, which is ascribed to the hole injection. In the final stress stage ($>10^4$ s), the saturation of the $G_m$ degradation stops and the $G_m$ degradation starts to increase again for ac stress, which is probably due to the hole traps accumulated at the interface.

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# A Triple-Beam 6.7 GHz, 340 kW Monotron

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***Abstract*—The low-voltage monotron oscillator described in this brief comprises a cylindrically symmetric cavity operating in the $TM_{040}$ mode, excited by three axially-directed hollow beams. The cavity geometry (radius 8.42 cm, length 1.0 cm) and injection beam energy (10 keV) are determined by a one-dimensional treatment disregarding space-charge forces. A 2.5-D particle-in-cell simulation is carried out for 0.4-cm thick beams at 80 A current giving 340 kW output power at an overall tube efficiency of 14.2%.**

***Index Terms*—Microwave generation, monotron, transit-time tubes.**

## I. INTRODUCTION

This brief addresses the monotron[1]–[3] in the low-current regime by examining its capabilities regarding electronic tuning and high-efficiency operation. These issues are considered in Section II, which shows that the discrete frequency spectrum of the monotron instability is determined by three parameters, namely, the interaction length, the injection beam energy, and the amplitude of the RF electric field. As a verification of the high-efficiency operating regime predicted by one-dimensional analysis, Section III describes a 2.5-D particle-in-cell simulation of a triple-beam $TM_{040}$, 6.7 GHz monotron where each beam is injected into the resonant cavity at 80 A current and 10 keV energy. Section IV reviews the present work and highlights the merits of the monotron with respect to the gyrotron.

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