Electronic Circuits Laboratory
EE462G
Lab #7

NMOS and CMOS Logic Circuits

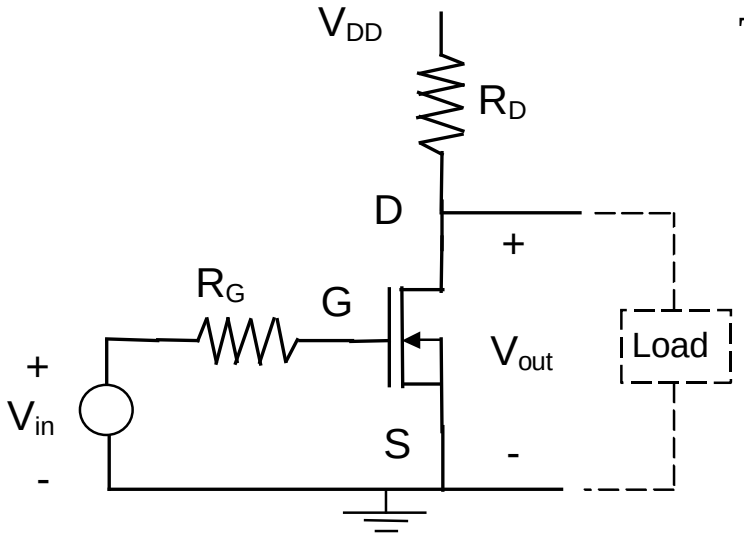
Logic Device Nomenclature

5-Volt Positive logic: Logic gate circuitry where a 5V level corresponds to logic 1 and 0V level corresponds to logic 0.

- **Truth Table:** Input-output description of gate in terms of logic symbols.
- $\mathbf{V_{IL}}$**:** Highest input voltage guaranteed to be accepted as a logic 0.
- $\mathbf{V_{IH}}$**:** Lowest input voltage guaranteed to be accepted as a logic 1.
- $\mathbf{V_{OL}}$**:** Highest logic-0 output voltage produced (given inputs are consistent with $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$).
- $\mathbf{V_{OH}}$**:** Lowest logic-1 output voltage produced (given inputs are consistent with $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$).

FET Operation as a Logic Device

Input values will change between 0 volts ($V_{GS} < V_{tr}$) and 5 volts ($V_{GS} > V_{DS}+V_{tr}$). Thus, the NMOS transistor will operate primarily in the cutoff and triode regions. The circuit below represents a logic inverter.



Three Regions of Operation:

Cutoff region ($V_{GS} \leq V_{tr}$)

Triode region ($V_{GS} > V_{tr}$, $V_{DS} \leq V_{GS} - V_{tr}$)

Constant current region

($V_{GS} > V_{tr}$, $V_{DS} > V_{GS} - V_{tr}$)

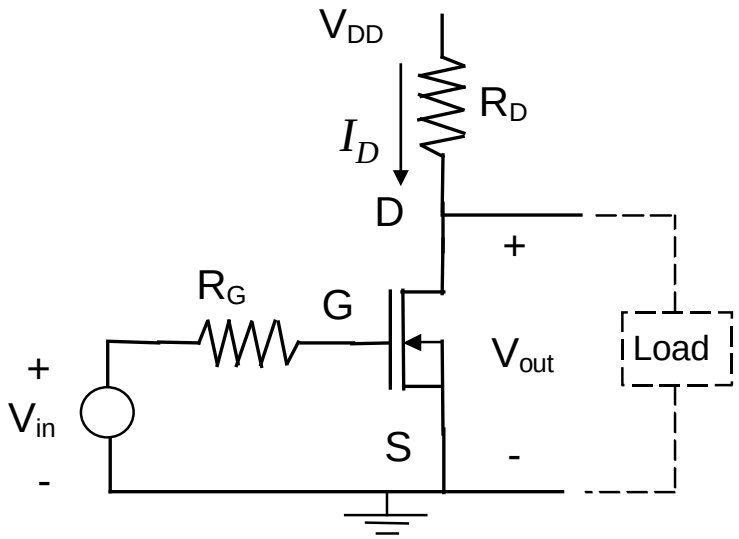
Triode region $I_D = Kp\left[2(V_{GS} - V_{tr})V_{DS} - V_{DS}^2\right]$

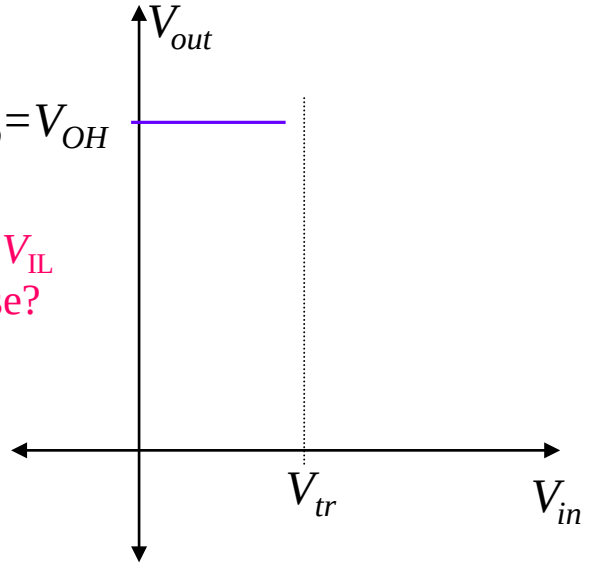
Transfer Characteristic

Obtain relationship between V_{in} to V_{out} in cutoff region.

$$V_{in} \approx V_{GS} < V_{tr} \longrightarrow I_D \approx 0$$

$$V_{DD} = R_D I_D + V_{DS} \longrightarrow V_{DD} \approx V_{DS} = V_{out}$$





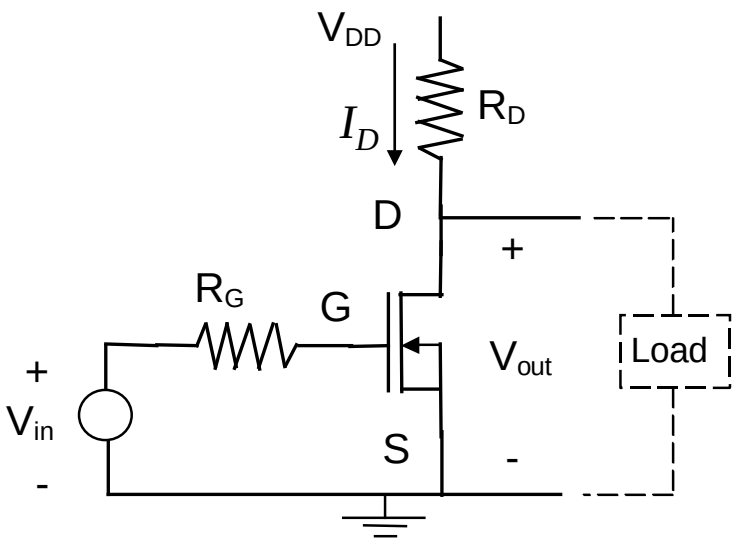
What would V_{IL} be in this case?

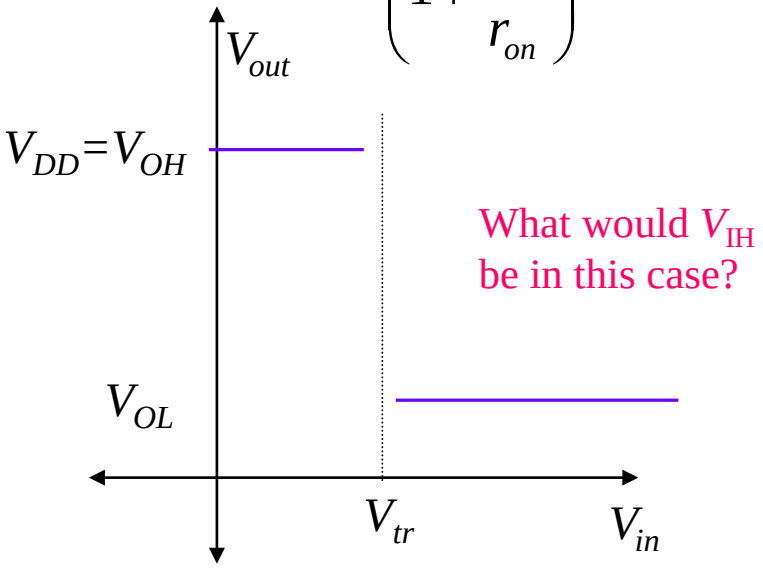
Transfer Characteristic

Obtain relationship between V_{in} to V_{out} in Triode region.

$$V_{in} \approx V_{GS} > V_{DS} + V_{tr} \longrightarrow I_D \approx Kp\left(V_{GS} - V_{tr}\right)V_{DS} = \frac{V_{DS}}{r_{on}} \quad \text{where} \quad r_{on} = \frac{1}{Kp\left(V_{GS} - V_{tr}\right)}$$

$$V_{DD} = R_D I_D + V_{DS} \longrightarrow V_{DD} \approx V_{DS}\left(1 + \frac{R_D}{r_{on}}\right) \longrightarrow V_{out} \approx \frac{V_{DD}}{\left(1 + \frac{R_D}{r_{on}}\right)} \approx V_{OL}$$

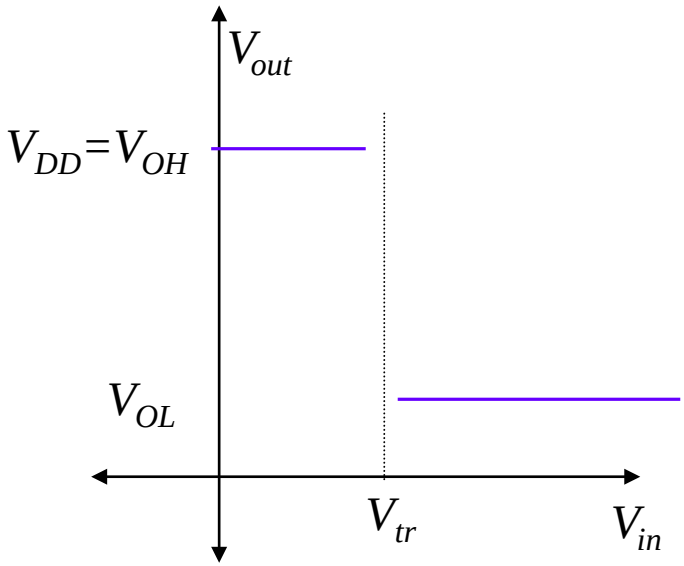




What would V_{IH} be in this case?

Truth Table

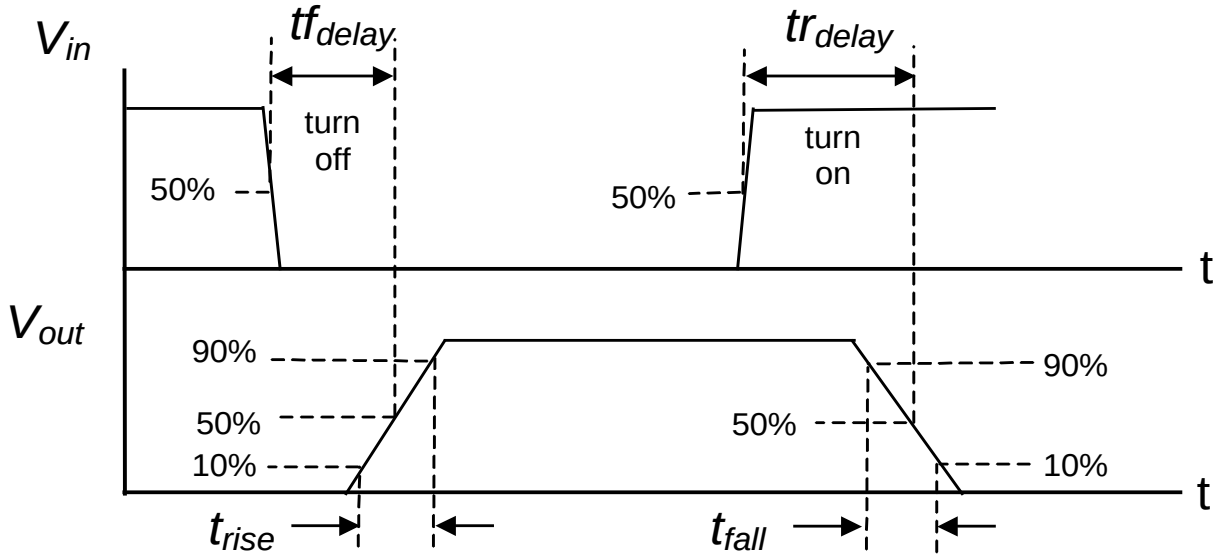
The truth table with logic input-output relationships are shown below:



Input	Output		V_{in}	V_{out}
0	1		$V_{IL} < V_{tr}$	$V_{OH} \approx V_{DD}$
1	0		$V_{IH} > V_{tr}$	$\frac{V_{DD}}{\left(1+\frac{R_D}{r_{on}}\right)} \approx V_{OL}$

Transition Between States

- The stray capacitance in the NMOS device limits the speed of the transition between states of the inverter.
- Capacitive effects between the drain and source, and gate and source create delays (propagation delay) between input and output transitions, and nonzero rise times and fall times of the output transitions.
- These quantities are defined below:



Propagation delay is taken as the average between the 2 edge delays

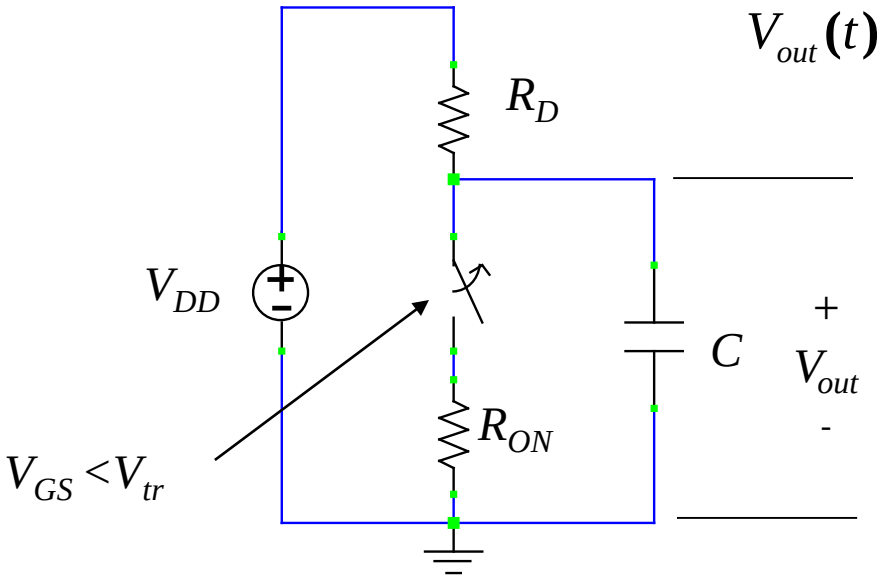
$$t_{PD} = \frac{tr_{delay} + tf_{delay}}{2}$$

Transition Low to High

- The equivalent circuit below represents the NMOS inverter going into a logic 1 output state.
- Circuit equations are:

$$V_{DD} = V_{out} + CR_D\dot{V}_{out} \qquad V_{out}(0^+) = V_{OL}$$

$$V_{out}(t) = V_{DD} - (V_{DD} - V_{OL})\exp\left(\frac{-t}{R_D C}\right)$$

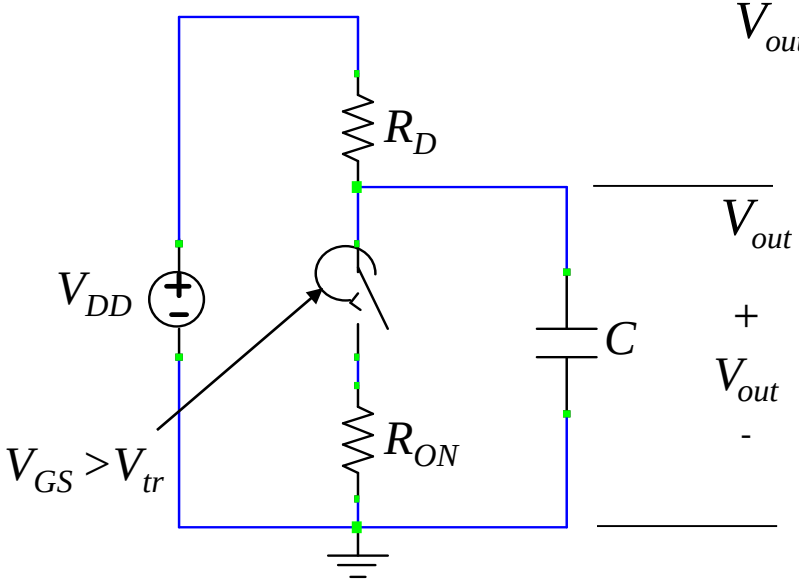


What critical parameters affect the rise time?
What effects would V_{DD} have on the rise time?

Transition High to Low

- The equivalent circuit below represents the NMOS inverter going into a logic 0 output state.
- Circuit equations are:

$$\frac{R_{ON}}{R_{ON}+R_D}V_{DD} = V_{out} + \frac{R_D R_{ON}}{R_{ON}+R_D}C\dot{V}_{out}$$



$$V_{out}(0^+) = V_{OH} \qquad V_{OL} = V_{DD}\frac{R_{ON}}{R_{ON}+R_D}$$

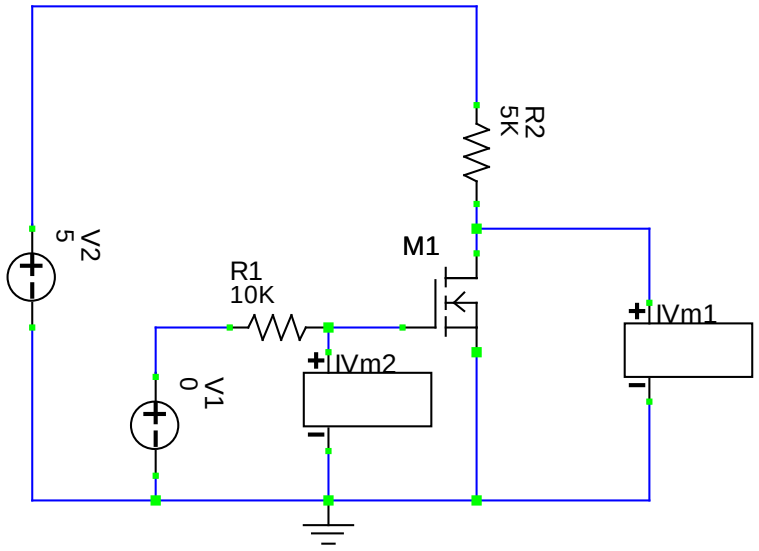
$$V_{out}(t) = V_{OL} - (V_{OL} - V_{OH})\exp\left(\frac{-t}{\frac{R_{ON}R_D}{R_{ON}+R_D}C}\right)$$

What critical parameters affect the fall time?

What effects would V_{DD} have on the fall time (note this ends in the triode region)?

SPICE Analysis

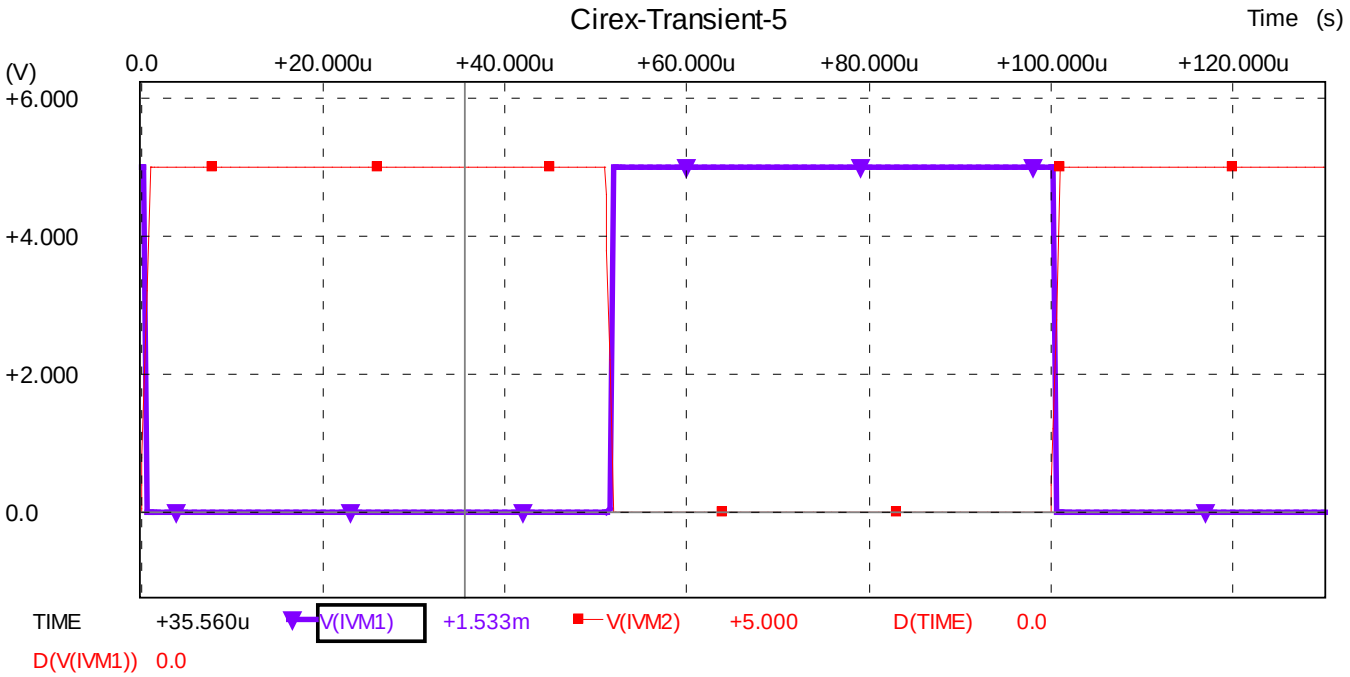
The logic circuit can be analyzed in SPICE. For this lab use the MOSFET (Level 1 NMOS) component model. This is a generic model where parameters such as *Kp* and V_{tr} can be set. Stray capacitance values can also be set; however, this lab does not request this.



The transient simulation can be run, using V2 as V_{DD} and V1 as a square wave (pulse setting in SPICE). The input and output voltages can be observed simultaneously.

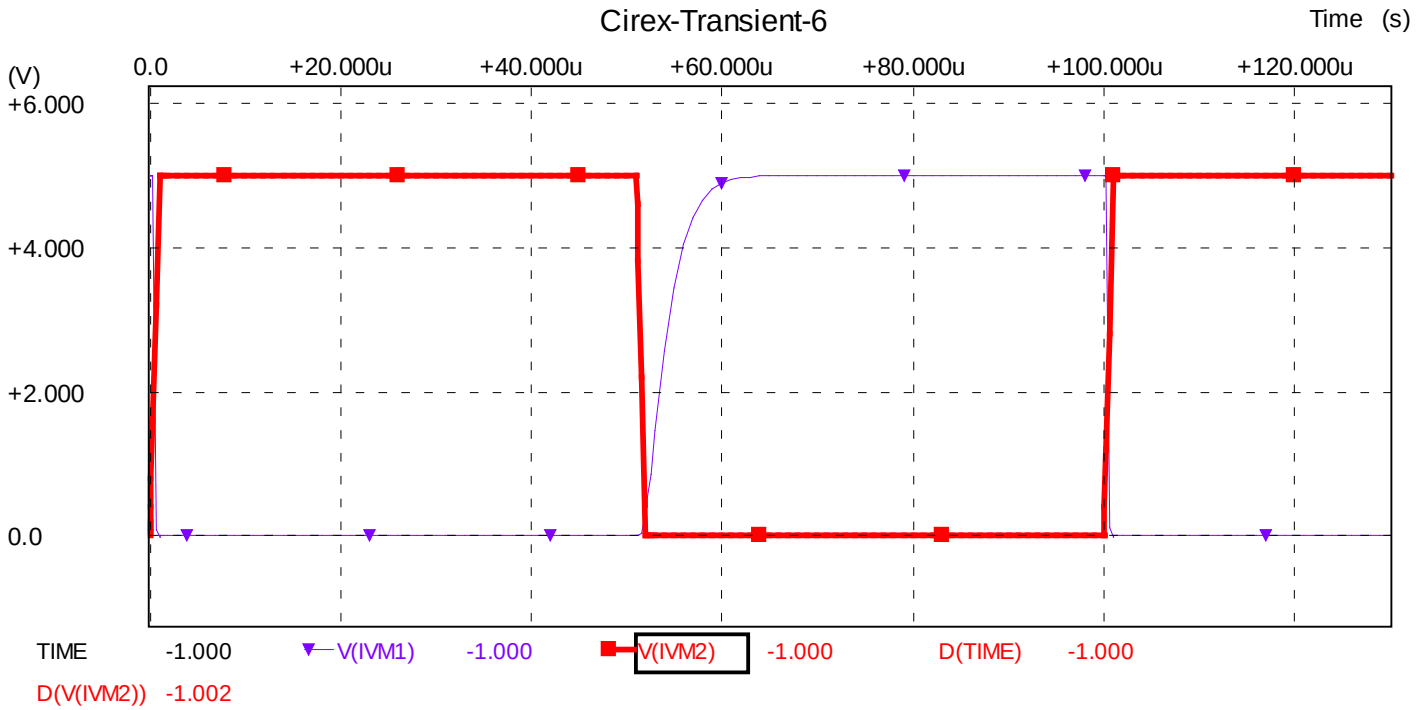
SPICE Results

Using a 10kHz square wave input, *Kp*=.225 and V_{tr} = 2.1:



SPICE Results

Using a 10kHz square wave input, *Kp*=.225 and V_{tr} = 2.1 and Drain-Body and Source-Body capacitance of 1nF each:



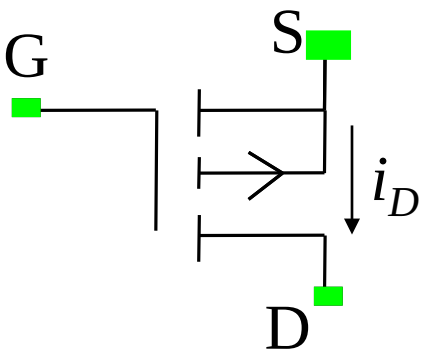
CMOS

Complementary metal-oxide semiconductor logic (CMOS) circuits use both NMOS and PMOS transistors. Desirable properties include:

- Zero static-power consumption.
- Smaller devices with thinner gate oxide leading to smaller propagation delays and lower supply voltages.
- Smaller chip areas as a result of eliminating resistors.

PMOS Characteristics

The p-channel MOSFET symbol and equations



Three Regions of Operation (Note that $V_{tr} \leq 0$):

Cutoff region $(V_{tr} \leq V_{GS})$

$(i_D = 0)$

Triode region $(V_{tr} \geq V_{GS})$ $(V_{DS} \geq V_{GS} - V_{tr})$

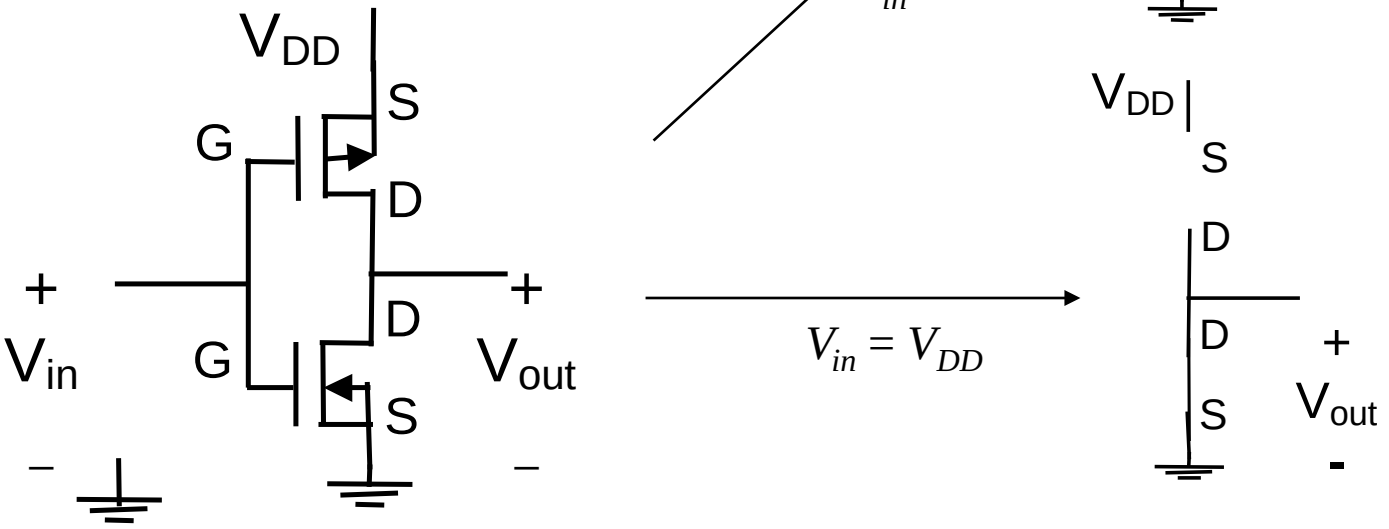
$$I_D = \left(\frac{W}{L}\right)\frac{KP}{2}\left[2(V_{GS} - V_{tr})V_{DS} - V_{DS}^2\right]$$

Constant current region $(V_{tr} \geq V_{GS})$ $(V_{GS} - V_{tr} \geq V_{DS})$

$$I_D = \left(\frac{W}{L}\right)\frac{KP}{2}(V_{GS} - V_{tr})^2$$

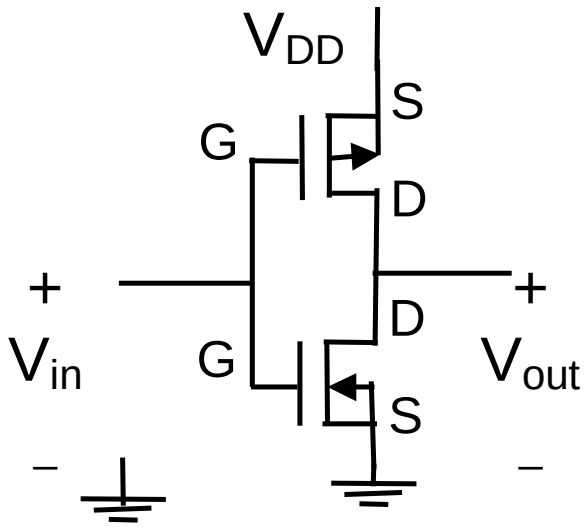
Ideal CMOS Inverter

Sketch the equivalent circuit by replacing the MOS transistors with short and open circuits when $V_{in} = 0$ and $V_{in} = V_{DD}$. Generate a truth table.



Transfer Characteristics

A load-line analysis is no longer possible in a CMOS circuit because the current-voltage relationship of the other transistor is not linear:



Equations for analysis:

$$V_{DD} = -V_{DSp} + V_{DSn}$$

$$V_{DD} = -V_{GSp} + V_{in} \qquad V_{GSn} = V_{in}$$

For constant current regions:

$$I_{DSn} = K_n (V_{GSn} - V_{trn})^2$$

$$I_{SDp} = K_p (V_{GSp} - V_{trp})^2$$

For triode regions:

$$I_{DSn} = K_n \left[2(V_{GSn} - V_{trn}) V_{DSn} - V_{DSn}^2 \right]$$

$$I_{SDp} = K_p \left[2(V_{GSp} - V_{trp}) V_{DSp} - V_{DSp}^2 \right]$$

Load-Curve Analysis

While the 2 circuit elements have non-linear *i-v* relationships, the intersection of their transfer characteristic curves, constrained by the circuit equations from KVL and KCL, yield the circuit voltages and currents.

The circuit constrains the relationship between the input voltage and gate voltages according to:

$$V_{GSp} = V_{in} - V_{DD} \qquad V_{GSn} = V_{in} \qquad V_{DSp} = V_{DSn} - V_{DD}$$

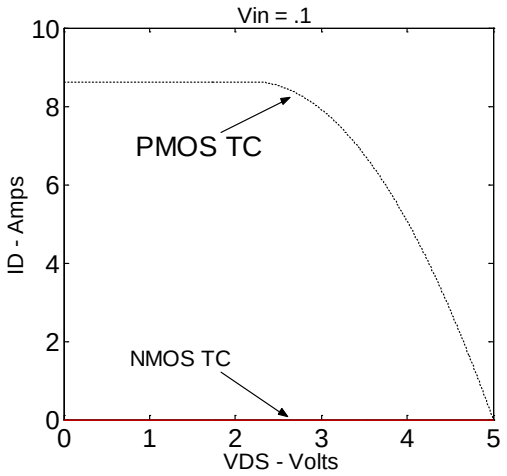
A Matlab program was written to sweep through values of V_{in} and find the operating points of the transistors. Note that for an open circuit load:

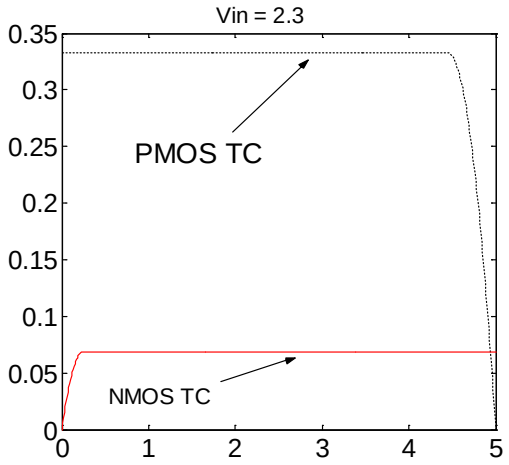
$$V_{out} = V_{DSn} \qquad I_{DSn} = I_{SDp}$$

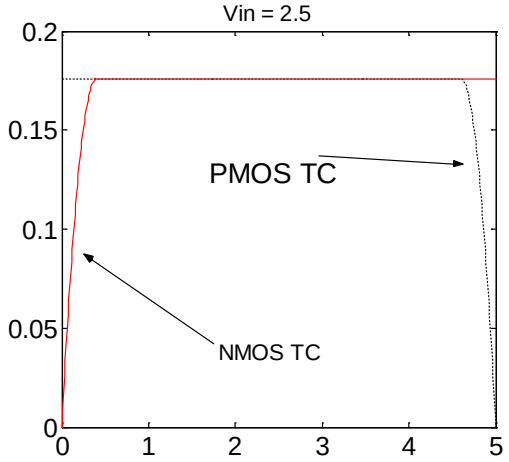
Program to Find TC of Circuit

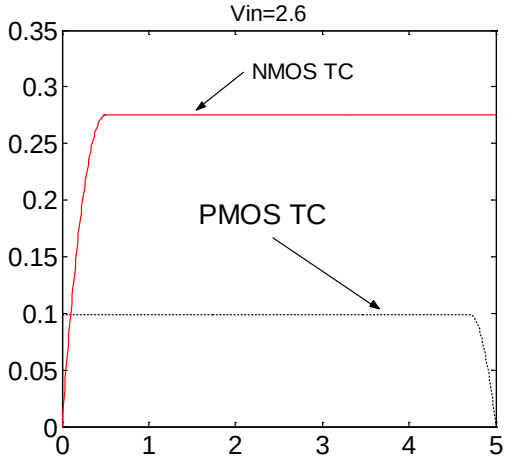
```
vton = 2.1;   %  Threshold voltage for NMOS
vtop = -2.1;  %  Threshold voltage for PMOS
K=1.1; W=1; L=1; KP=2*K;  VDD=5;
vin = [0:.05:VDD];  % input voltages to sample at
vdsn = [0:.01:VDD];  %  Create Vds value over of the NMOS transistor
vdsp = vdsn-VDD;  %  Create vds values over the PMOS transistor (note vsdn-vdsp=VDD)

%  Loop to compute operating points
for vinx = 1:length(vin)
      idsp = pmos(vdsp,vin(vinx)-VDD,KP,W,L,vtop);  %  Generate Load Curve (gate voltage is vin-VDD)
       idsn = nmos(vdsn,vin(vinx),KP,W,L,vton);  % Compute characteristic curve
%  get effective intersection point
       [err, inderr] = min(abs(idsp - idsn));  %  Find closest point
   vout(vinx) = vdsn(inderr(1));  %  Store output voltage
   id(vinx) = idsp(inderr(1));       %  Store drain current
end
```

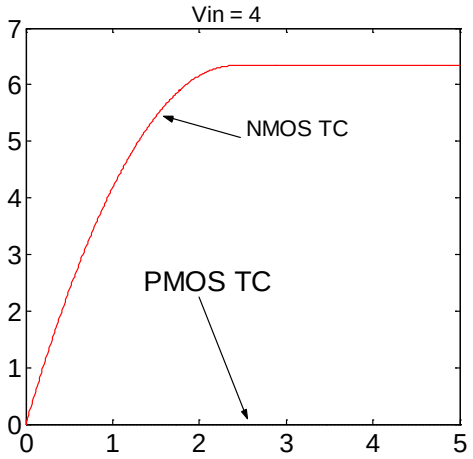
TCs for Various V_{in} Values







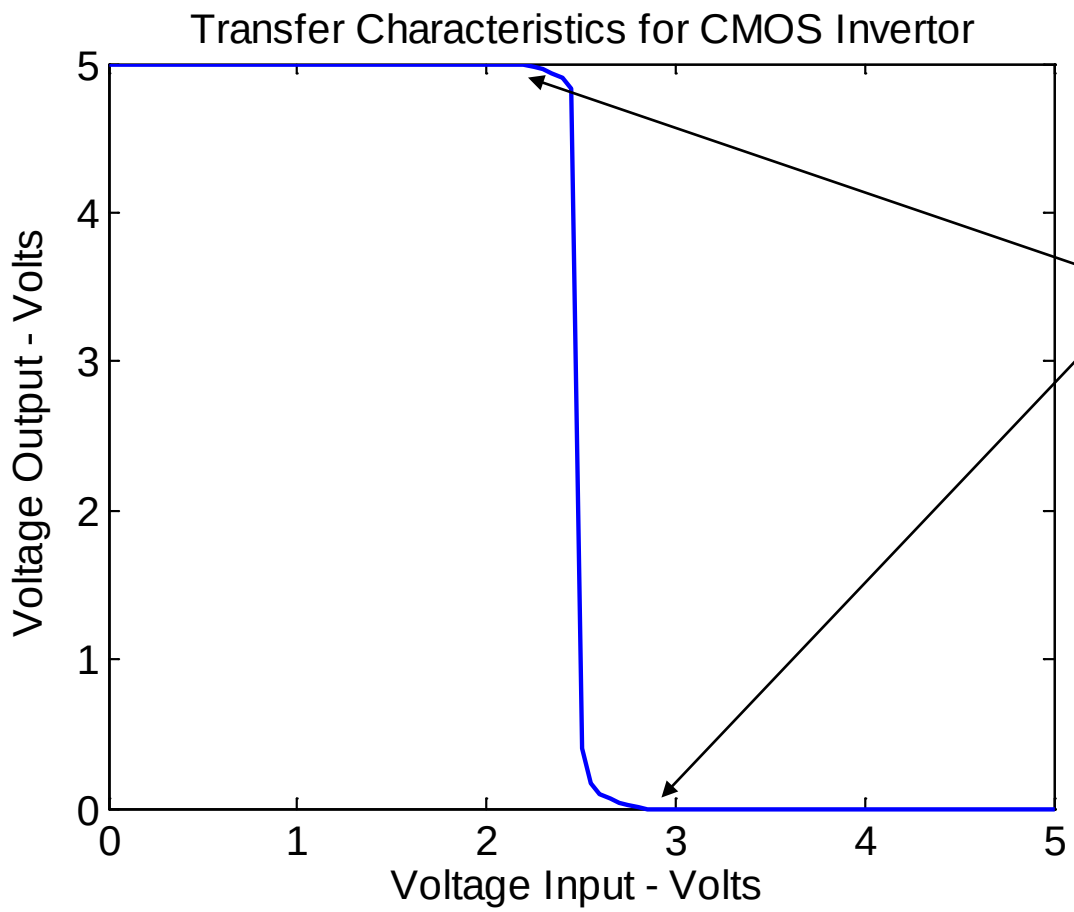




Note that the PMOS TC is mapped from V_{DSp} to V_{DSn} through the KVL equation

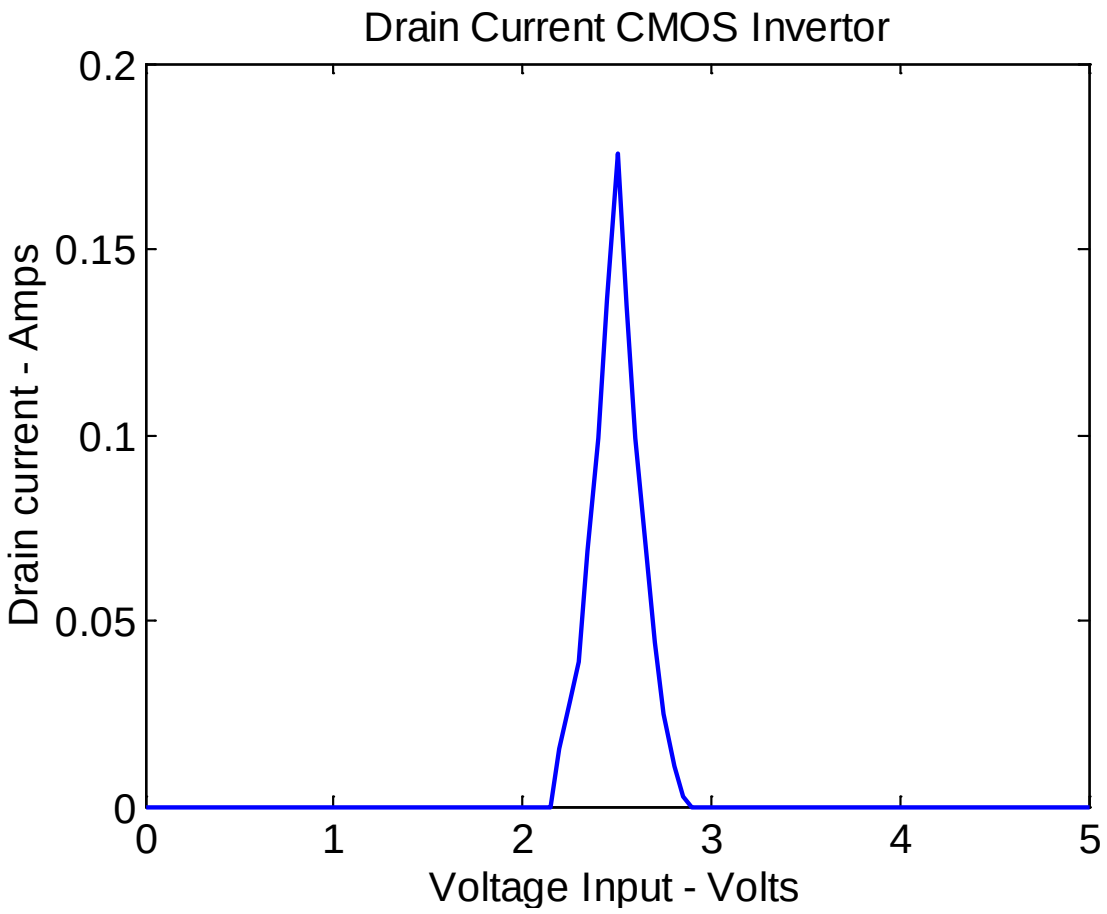
$$V_{DSn} = V_{DSp} + V_{DD}$$

TC: V_{out} vs. V_{in}

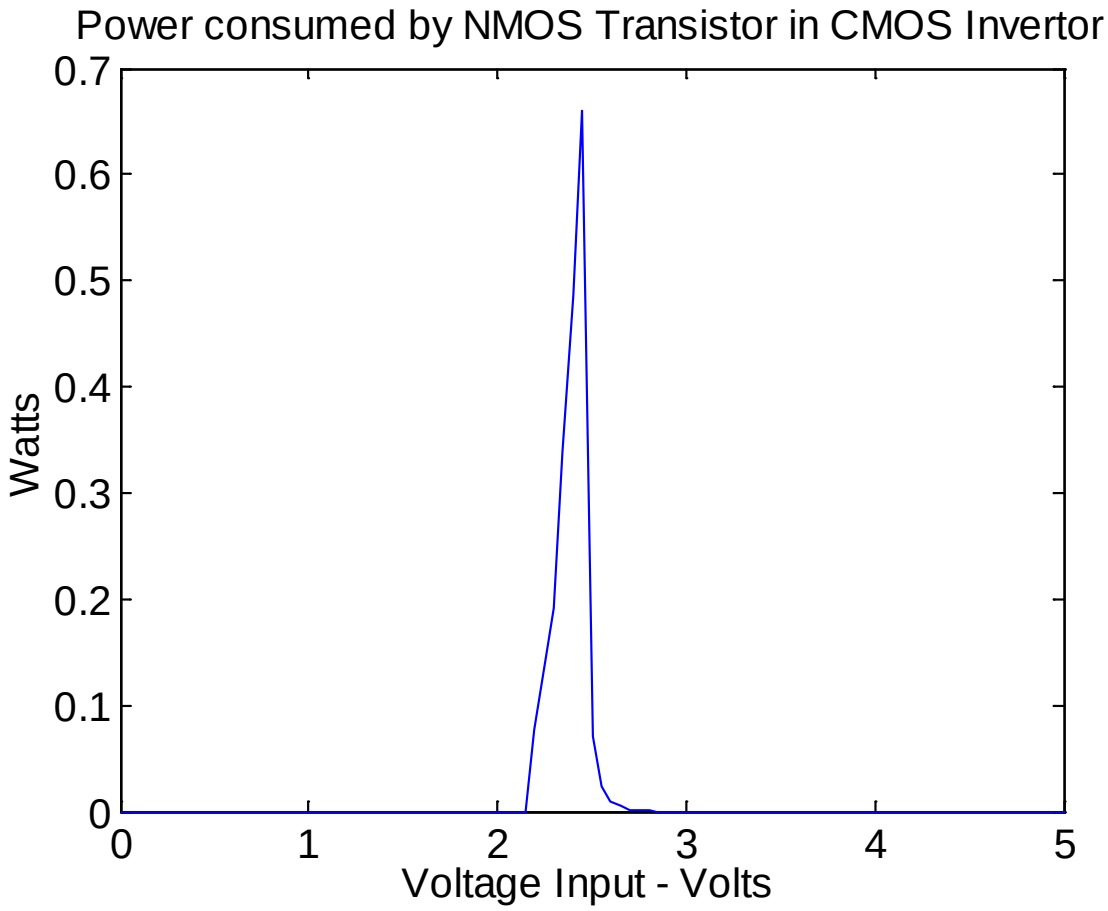


Threshold Voltage effect

TC: I_{DS} vs. V_{in}

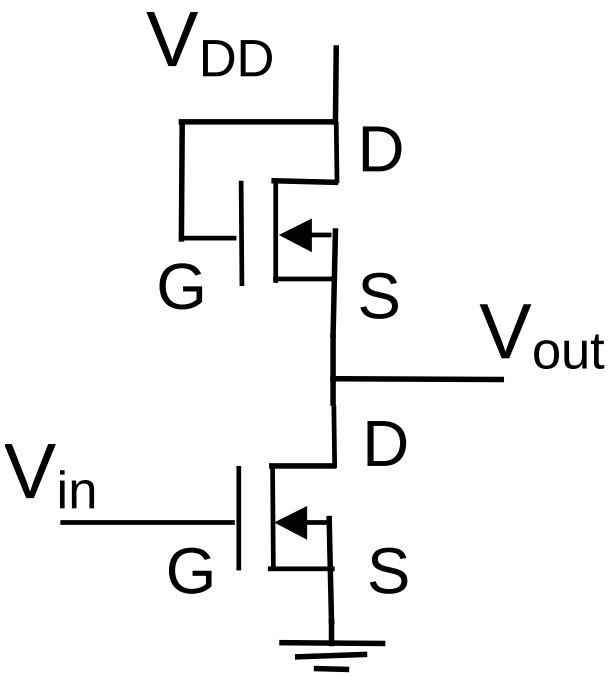

Drain Current CMOS Invertor
Drain current - Amps
0.2
0.15
0.1
0.05
0
0
1
2
3
4
5
Voltage Input - Volts

TC: Instantaneous Power vs. V_{in}



How does this curve demonstrate zero static power consumption?

NMOS Logic Inverter Circuit



This circuit will be examined in the lab. Note the "diode-connected" NMOS transistor. Determine the TC of this connection.

$$V_{DS} = V_{GS}$$

This ensures the operation is either in the cutoff or con atant current region:

$$V_{DS} \geq V_{GS} - V_{tr} \quad \text{or} \quad V_{tr} \geq V_{GS}$$

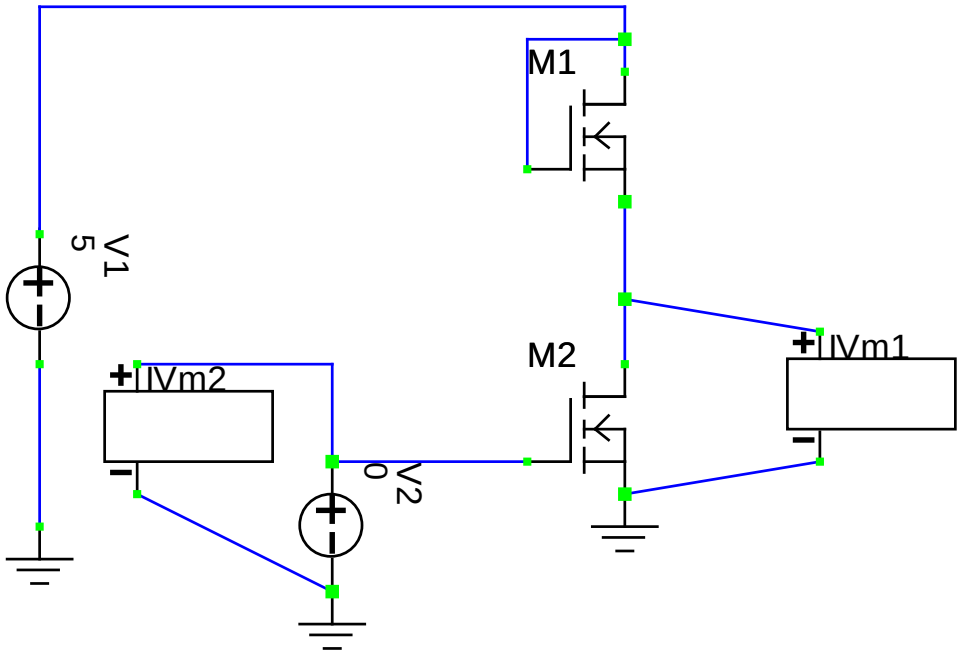
$$I_D = Kp\left[2(V_{GS} - V_{tr})V_{DS} - V_{DS}^2\right]$$

SPICE Example

Compare input and output of inverter using a 10kHz square wave input, with a level 1 nmos fet setting *Kp*=.225, *Vtr* = 1.8 and Drain-Body and Source-Body capacitance of 0.1μF each:

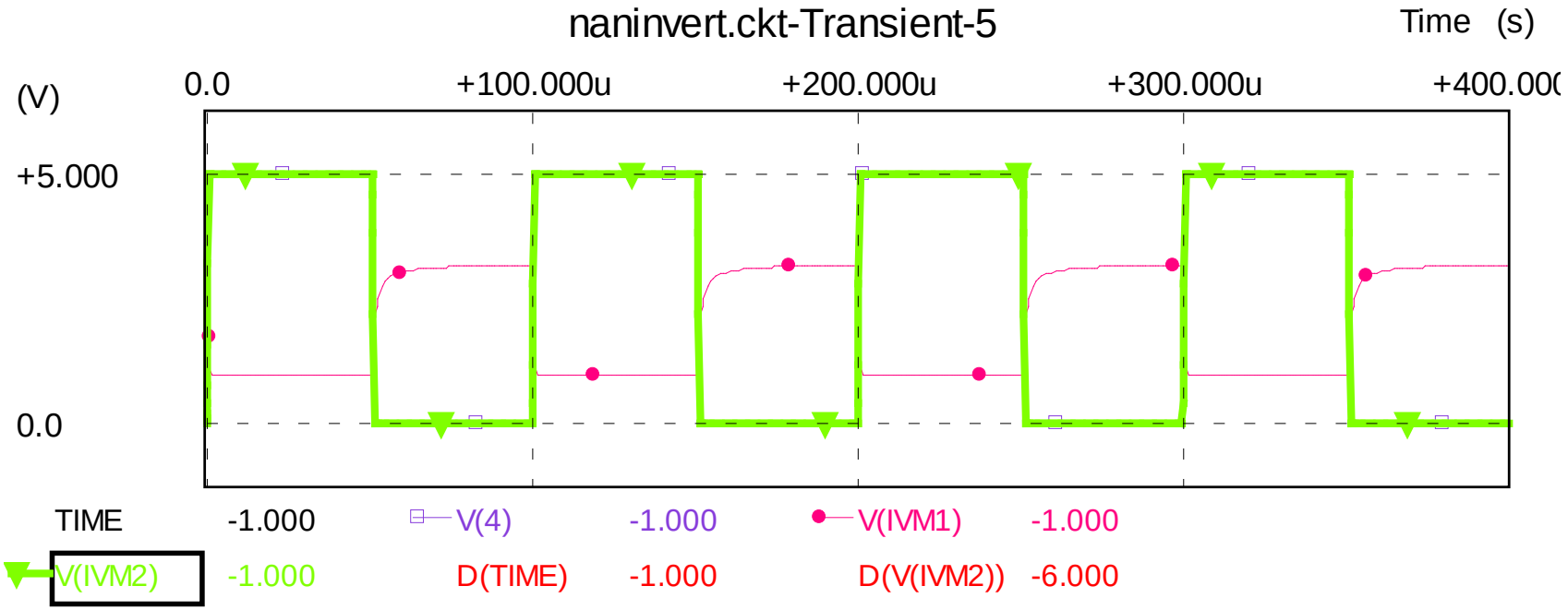
In SPICE use the pulse input for V2 and set transient properties with appropriate period and voltage levels.

For the FET, edit simulation properties and select the shared properties tab to set the parameters.



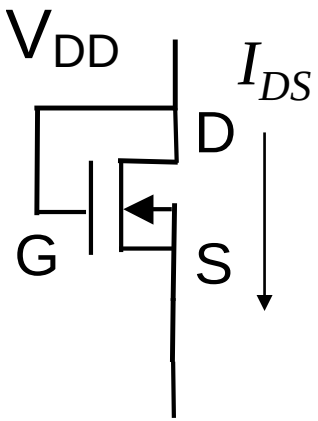
SPICE Result

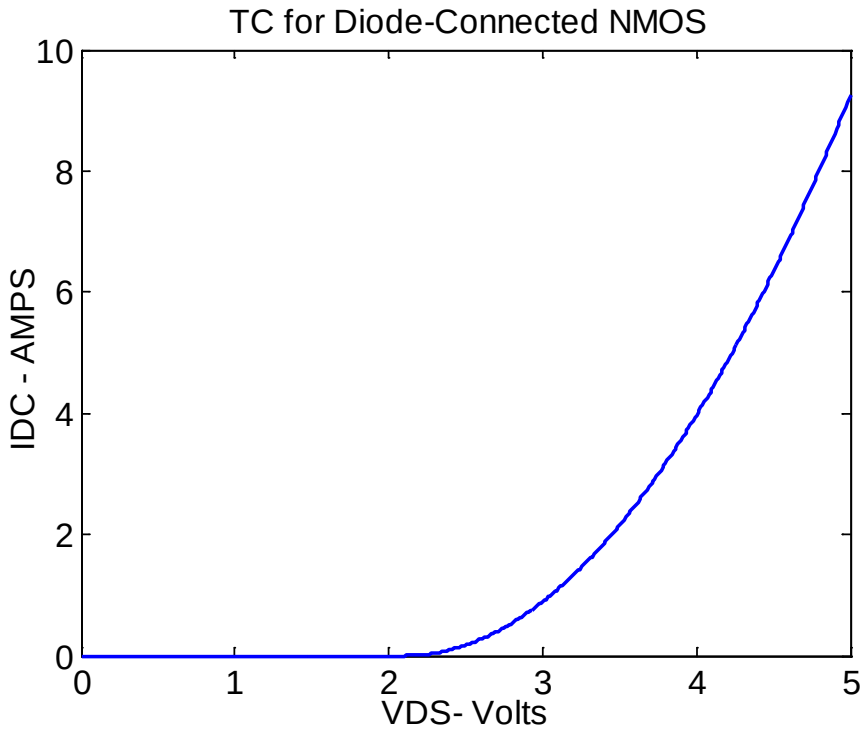
(Input fat/green, Output skinny/red) Note capacitive effects and results of using the NMOS transistor as a pull-up resistor.



TC of Diode-Connected NMOS

```
vton = 2.1;   %  Threshold voltage for NMOS
K=1.1; W=1; L=1; KP=2*K;  VDD=5;
vdsn = [0:.01:VDD];  %  Create Vds value over of the NMOS transistor
vgs = vdsn;  % input voltages to sample at

%  Loop to compute operating points
for k = 1:length(vgs)
    % Compute characteristic curve
    idsn(k) = nmos(vdsn(k),vgs(k),KP,W,L,vton);
end
```



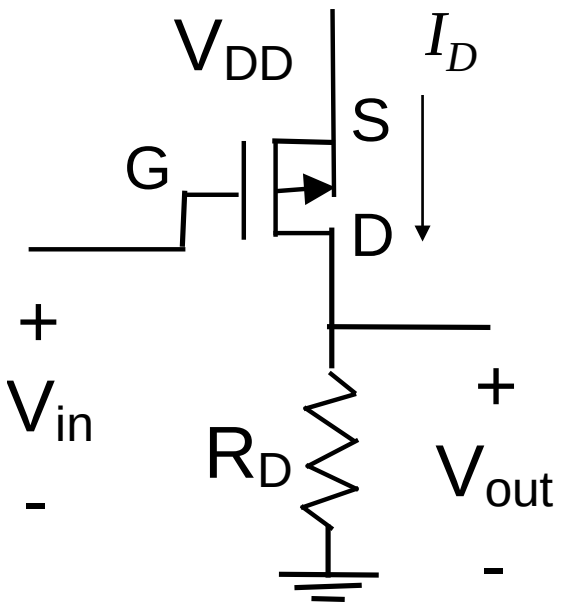


PMOS Characterization Circuit

Use Matlab to compute TC of circuit

$$V_{GSp} = V_{in} - V_{DD} \qquad I_D = \frac{V_{DS} + V_{DD}}{R_D}$$

Let R_D = 5kΩ, V_{DD} = 5V, and sweep V_{in} from 0 to 5V




```
%  Set Parameters
K=.15; vto = -2.1;
W=1; L=1; KP=2*K;
VDD=5;   RD=5000;
vds = -[0:.001:VDD];  %  sample point for load line and TC
vin = [0:.01:VDD]; %  Create x-axis
idsll = vds/(RD) + VDD/(RD);  %  Generate Load Line
%  Loop to sweep through input values
for k=1:length(vin)
   ids = pmos(vds,vin(k)-VDD,KP,W,L,vto);  % Compute characteristic curve
   [err, inderr] = min(abs(idsll - ids));  %  Find closest point to desired operating point
   vout(k) = idsll(inderr(1))*RD;    %   Compute output voltage
   id(k) = idsll(inderr(1));              %   Store drain current in array
end
```

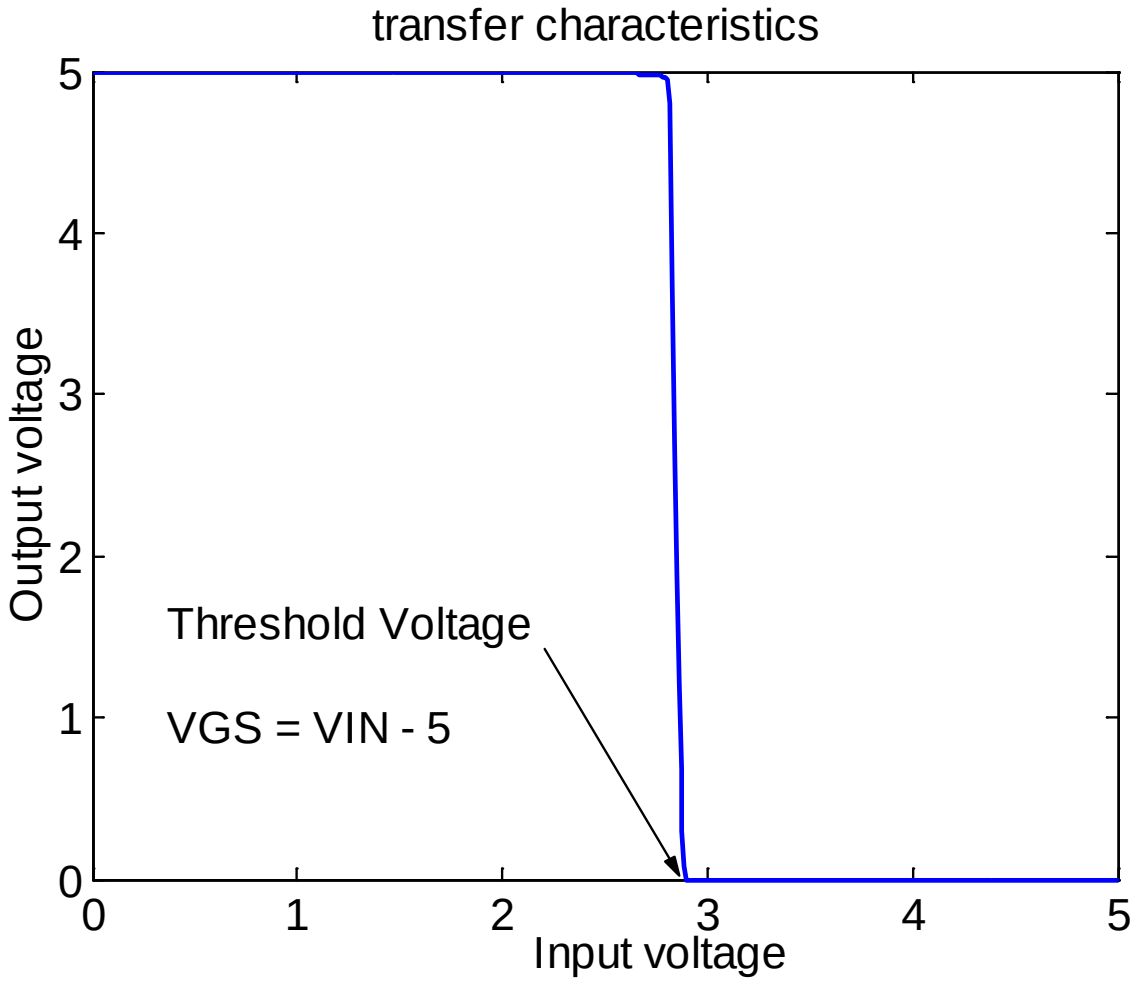
PMOS TC Mfile Function

```
function ids = pmos(vds,vgs,KP,W,L,vto)

%  This function generates the drain-source current values "ids" for
%  a PMOS Transistor as a function of the drain-source voltage "vds".
%
%    ids = nmos(vds,vgs,KP,W,L,vto)
%
%    where "vds" is a vector of drain-source values
%               "vgs" is the gate voltage
%               "KP" is the device parameter
%               "W" is the channel width
%               "L" is the channel length
%               "vto" is the threshold voltage
%   and output "ids" is a vector of the same size of "vds"
%   containing the drain-source current values.

ids = zeros(size(vds));  %  Initialize output array with all zeros

k = (W/L)*KP/2;   %  Combine devices material parameters
```

PMOS TC Mfile Function

```
%  For non-cutoff operation:
if vgs <= vto
      %  Find points in vds that are in the triode region
      ktri = find(vds>=(vgs-vto) & vds <= 0);  %  Only take point up to the gate voltage minus the threshold.
      %  If points are found in the triode region compute ids with proper formula
      if ~isempty(ktri)
         ids(ktri) = k*(2*(vgs-vto).*vds(ktri)-vds(ktri).^2);
      end
      % Find points in saturation region
      ksat = find(vds<(vgs-vto) & vds <= 0);   %  Take points greater than the excess voltage
      %  if points are found in the saturation regions compute ids with proper formula
      if ~isempty(ksat)
         ids(ksat) = k*((vgs-vto).^2);
      end
   %  If points of vds are outside these ranges then the ids values remain zero
end
```

TC: PMOS Circuit



Questions for Lab Report:

- What is the purpose of decoupling capacitors (in parallel with the DC power supply) in CMOS logic circuits?

- What factors determine the highest clock speed at which a logic gate can reliably be driven?