Review of Ch. 6 & Ch. 7

Ch. 6

General structure of an inverter

BJT inverter: Diagram.

How to obtain transfer characteristics ?

Mathematically: (1) Base - Emitter loop → Solve to obtain i_B

Use $i_C = \beta_F i_B$ to obtain i_C

(2) Collector - Ground loop: obtain V_{out}

(3) Draw $V_{out} \sim V_{IN}$ curve

Graphically: (1) Draw the BJT i-V curves

(2) Draw load line: $i_x \sim V_{OUT}$

(3) Draw $V_{out} \sim V_{IN}$ curve base on

$$V_{IN} = i_B R_B + V_f$$

$$\text{Gain} = \frac{d V_{OUT}}{d V_{IN}} \quad \text{or} \quad \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

MOSFET inverter: Diagram

How to obtain transfer characteristics ?

Mathematically: (1) Find i_D: $i_D = K(V_{IN} - V_{TR})^2$ for CCR

(2) V_{DD} - Ground Loop: obtain V_{out}

(3) Draw $V_{OUT} \sim V_{IN}$ curve

Graphically: (1) Draw MOSFET i-V curves

(2) Draw load line

(3) Draw $v_{OUT} \sim v_{IN}$ curve based on

$$v_{IN} = \sqrt{\frac{i_D}{k}} + V_{TR}$$

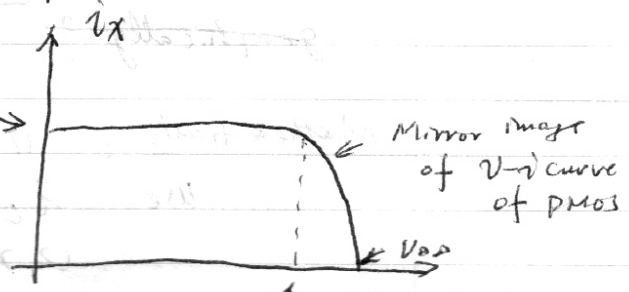
$$\text{Gain} = \frac{dv_{OUT}}{dv_{IN}} \doteq \frac{\Delta v_{OUT}}{\Delta v_{IN}}$$

CMOS inverter: R_D replaced with a P-MOSFET

Key: How to draw the loadline?

loadline: $i_X \sim v_{OUT} = V_{DD} - V_p$

$$i_X = -i_{DP} = -K_p (v_{GSP} - V_{TRP})^2$$



Once you have loadline, you can follow the same procedure as above to obtain the transfer characteristics.

BJT Voltage follower:

Diagram

Obtain $v_{OUT} \sim v_{IN}$ { accurately / approximately if $(\beta_F + 1) R_E >> R_B$

in three regions: CCR, cut-off, Saturation

MOSFET voltage follower:

Diagram

Obtain v_{OUT} vs. v_{IN} in CCR

BJT logic inverter:

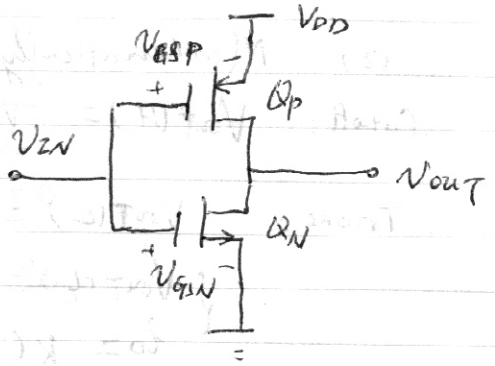
Diagram

To be able to draw transfer characteristics schematically with right labels. What are the disadvantages?

Digital

CMOS Inverter:

Diagram



Schematically understanding the output vs. input

Be able to draw the transfer characteristics schematically with labels.

Be able to calculate V_{ZC}, power consumption.

Ch. 7

Biasing for BJT:

$V_{OUT} = \frac{V_{OUT(L)} + V_{OUT(H)}}{2}$; V_{sat} ↙ V_{CC} — midpoint of two limits

Find $V_{BB} \sim V_{OUT}$

$$V_{BB} = \left(\frac{V_{CC} - V_{OUT}}{\beta_F}\right)\frac{R_B}{R_C} + V_f$$

Feedback biasing of BJT:

Given V_{BB}:

Input loop: obtain I_B. $I_C = \beta_F I_B$.

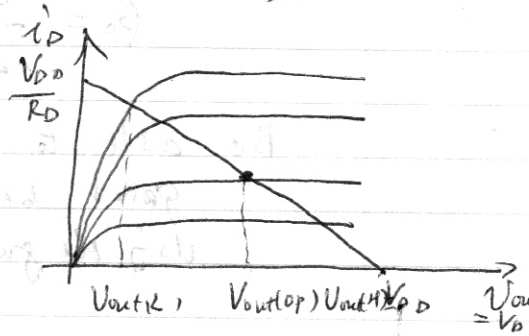
Output loop: obtain V_{CE}

If $(\beta_F + 1) R_E >> R_{BB}$, $I_C \simeq \frac{V_{BB} - V_f}{R_E}$

$$V_{CE} \simeq V_{CC} - I_C (R_C + R_E)$$

Biasing for MOSFET:

1) Graphically:



(2) Mathematically,

Cutoff: $V_{OUT}(H) = V_{DD}$, $i_D = 0$ ✓ beginning of CCR

Triode: $V_{OUT}(L) = ?$ $\qquad V_{OUT}(L) = (V_{GS} - V_{TR})$

$$\begin{cases} V_{OUT}(L) = V_{DD} - i_D R_D \\ i_D = K(V_{GS} - V_{TR})^2 = K[V_{OUT}(L)]^2 \end{cases}$$

$$\Rightarrow V_{OUT}(L) = \frac{\sqrt{1 + 4KR_D V_{DD}} - 1}{2K R_D}$$

Bias:
$$\begin{cases} V_{OUT} = \dfrac{V_{OUT}(L) + V_{OUT}(H)}{2} \\ I_D = \dfrac{V_{DD} - V_{OUT}}{R_D} \\ V_{GS} = V_{TR} + \sqrt{\dfrac{I_D}{K}} \end{cases}$$

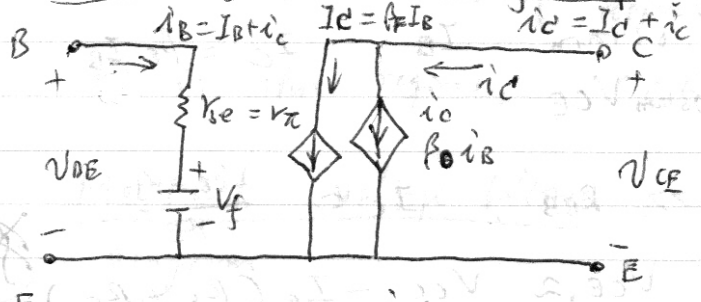
Feedback biasing of MOSFET:

Given V_G

(1) Find I_D from $\begin{cases} V_{GS} = V_G - I_D R_S \\ I_D = K(V_{GS} - V_{TR})^2 \end{cases}$

(2) Find V_{DS} & V_{GS}:

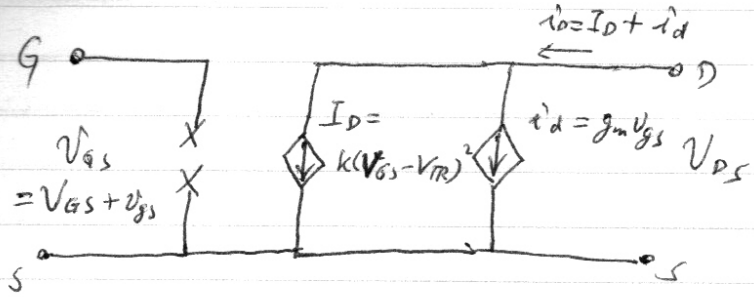
Small signal Model of BJT:



$$\beta_o = \frac{\Delta i_C}{\Delta i_B} \qquad \beta_F = \frac{I_C}{I_B}$$

Be able to find output signal and small signal gains based on the above model (set DC source = Zero) using the guideline.

Small signal model of FET:



$$g_m = \begin{cases} 2k(V_{GS} - V_{TR}) \\ 2\sqrt{k I_D} \end{cases}$$

Graphically : $g_m = \dfrac{\Delta i_D}{\Delta V_{GS}}$

Be able to find output signal and small signal gains using the guideline.