 Dec. 18, 2007
To be published at http://www.engr.uky.edu/~zhichen/

Recipe for Observation of Leakage Current Reduction due to Phonon-Energy Coupling Enhancement

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Supplement to the Following Publications:

1. **Z. Chen**, P. Ong, and C. B. Samantaray, "Large Leakage Current Reduction of Silicon Oxide and High-K Oxides Using the Phonon-Energy-Coupling Enhancement Effect," Abstract, 2007 International Semiconductor Device Research Symposium, Dec. 12-14, 2007, College Park, MD.
2. **Zhi Chen**, "Mechanism for Generation of the Phonon-Energy-Coupling Enhancement Effect for Ultrathin Oxides on Silicon," Appl. Phys. Lett. 91, 223513 (2007).
3. Pangleen Ong and **Zhi Chen**, "Evidence of enhanced phonon-energy coupling in SiO_2/Si," Appl. Phys. Lett. 90, 113516 (2007).
4. Chandan. B. Samantaray and **Zhi Chen**, "Reduction of Gate Leakage Current of HfSiON Dielectrics through Enhanced Phonon-Energy Coupling," Appl. Phys. Lett., vol. 89, 162903 (2006).
5. **Z. Chen** and J. Guo, "Dramatic reduction of gate leakage current of ultrathin oxides through oxide structure modification," Solid-State Electronics, vol. 50, 1004–1011 (2006).
6. **Z. Chen**, J. Guo, and F. Yang, "Phonon-energy-coupling enhancement: Strengthening the chemical bonds of the SiO_2/Si system," Appl. Phys. Lett. vol. 88, no. 8, 082905, 2006.

RECIPE

Oxidation

RCA cleaning and HF etching in the last step
Load samples at 900 ^{o}C in quartz furnace with 1000 sccm N_2
Thermal oxidation in 2% O_2 (O_2=20sccm and N_2=1000 sccm) at 900°C for 10s
Thickness measurement using ellipsometery (~22 Å)

Note: One may also use industrial oxynitride wafers with EOT=15Å, instead of oxidation.

Rapid thermal processing (RTP)

Key-factor: Slight oxide regrowth (1-2Å) at very high temperature

Introducing ~0.2% O_2 in N_2 (or He) during RTP
Ramp-up to 1100-1120°C at 10°C/s
Hold at 1100-1120°C for 45 s
Cooling down at the fastest rate of the RTP machine (~7s from 1100°C to 750°C in N_2)
Measurement of oxide thickness using ellipsometry: ~**2Å oxide regrowth** (or ~24Å)

Note: Three important factors: temperature, regrowth, and cooling rate. One may control the regrowth thickness by varying O_2 concentration and RTP time.

Front Contact

Method 1:
E-beam evaporation of ~1000Å-thick Ni layer on top of the oxide using a shadow mask to form circular Ni dots

OR

Method 2:
Patterning top electrodes for lift-off using a bi-layer resist procedure (Shipley S1813/SU-8 2001) (See the attached document, "Lithographic Procedure for Ni Gate Patterning Using Bi-Layer Resist")
E-beam evaporation of ~900Å -thick Ni layer at ~1Å/s
Lift off in SU8 PR remover (Remover PG) at 100-110°C for 45-60 min
Ultrasonic agitation 5s
Rinse in IPA

Back contact and anneal

Covering the front electrodes using positive photoresist (Shipley 1813)
Hard baking at 140°C for 2 min.
Etching the back oxide in buffered oxide etch (BOE) for 30 s
Thermal evaporation of ~1000Å thick Al on the backside
Removal of the positive PR using PR remover (Shipley 1165)
Forming gas anneal (10% H_2) at 450°C for 30 min.

Expected Results: Three orders of magnitude leakage current reduction

Note:

1. Refer to the key paper: **Z. Chen**, "Mechanism for Generation of the Phonon-Energy-Coupling Enhancement Effect for Ultrathin Oxides on Silicon," Appl. Phys. Lett. 91, 223513 (2007).
2. After RTP, do not use the OH-based chemicals including positive PR developer directly on oxides; do not expose oxides to plasma; do not expose the samples in air (moisture) for over 15 days. All these will cause partial loss of the PECE effect.
3. SU-8 developer is organic, which is not harmful to the PECE effect.
4. The new process using Ni gate allows us to do post-metal anneal so that correct C-V curves can be obtained.
5. Check any update in my website: http://www.engr.uky.edu/~zhichen/

Future development:

Developing fabrication processes compatible with the CMOS manufacturing.