



**NECP: Nanoscale Engineering Certificate Program
Department of Electrical & Computer Engineering
Center for Nanoscale Science and Engineering
University of Kentucky**



Spring 2006 Seminar Series

Micro and Nanotechnology Circuits – The Interconnect Problem

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Interconnects are mostly metallic lines used to connect transistors and other devices on an integrated circuit chip. On-chip interconnects contribute much more to the chip's overall propagation delay than that caused by the once dominant gate capacitances in transistors. Over the years, researchers have tried to reduce this delay by reducing the interconnect RC time constant. However, ever increasing frequencies, scaling of minimum feature sizes, the reduction of resistances and capacitances have all led to a growing dominance of on-chip inductances.

Formation of digital nanocomputers that promise dramatically increased computational speed and density requires the successful formation of molecular-scale devices. Even after the challenges of fabricating the molecular devices are successfully overcome, we still face the problem of connecting these devices in a circuit to carry the information from the output of one device to the input of the next device. The interconnect problem arises because of the extremely high density of devices in the circuit and because of the extremely high rapidity at which the information needs to be transmitted from one point to the next. This requires an unprecedented high density of interconnects operating at extremely high speeds.

April 26, 2006 (Wednesday)

ECE Conference RM, 453F Anderson Tower

3:00-4:00 pm