Easy Eldo Simulation Using
run_eldo_on_cell.rb

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Why use `run_eldo_on_cell.rb`?

- To easily run eldo
- To compare layout extracted sim to schematic sim
- To simulate one bias condition across process corners and/or temperature
- To simulate one bias condition on multiple cells
Setting up a simulation directory

• Why do you need a simulation directory?
  • `run_eldo_on_cell.rb` uses input files to get all the information needed to extract the netlists and create the eldo simulation files
  
  • Having properly named files reduces the number of command line options needed when executing
  
  • Easy to re-run simulations
Setting up a simulation directory

**Required run_eldo_on_cell.rb Files**

- **inc_list**
  - Contains path to models to use per library
- **eldo_opt_file**
  - Contains options for the eldo simulation

**bias_list**
- Contains bias conditions for the pins of the cells

**cell_list**
- Contains library, cell, temp, corner, IC to be simulated

**readout_pins**
- Contains list of pins that will be measured

SEE APPENDIX A FOR SAMPLE FILES
Setting up a simulation directory - Required Files

- **Sample Files**
  - A copy of all required files can be found at:
    
    /proj/module_automation/golden/module_automation/ruby/run_eldo_on_cell_files

- **Rarely Edited Files**
  - *inc_list*
    - Copy from link above
    - One time addition of library and models
  - *eldo_opt_file*
    - Copy from link above
    - Generic Eldo option file, all lines get copied into .cir file

SEE APPENDIX A FOR SAMPLE FILES
## Setting up a simulation directory - Required Files

### Frequently Edited Files

<table>
<thead>
<tr>
<th>File Name</th>
<th>Controls</th>
<th>Reason To Change</th>
<th>Impacts</th>
</tr>
</thead>
<tbody>
<tr>
<td>readout_pins</td>
<td>Which pins in netlist get reported by eldo</td>
<td>Change pins measured by eldo</td>
<td>.chi file</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>.tr0, .sw0, .ac0 files</td>
</tr>
<tr>
<td>bias_list</td>
<td>Analysis Type</td>
<td>Change Analysis (Single Point, DC Sweep, Transient)</td>
<td>Simulation settings in .cir file</td>
</tr>
<tr>
<td></td>
<td>Bias Conditions</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cell_list</td>
<td>Cells to simulate Corner Model Temp IC Model</td>
<td>Add/remove cells from simulation</td>
<td>Cells that are simulated w/ execution of script</td>
</tr>
</tbody>
</table>
Command Line Options

• **General Options**
  - `-RC_load <path to file>`
    - Use to simulate R & C loading effects
  - `-no_layout`
    - Use to perform schematic simulation only
  - `-useDDC`
    - Use to force a specific DDC in storing simulation results
  - `-FFT`
    - Perform FFT on pins specified in `readout_pins` file for frequency range of 0-10 GHz

• **Schematic Simulation Options**
  - `-netlist_par <path to file>`
    - Use to simulate a parameterized schematic

SEE APPENDIX A FOR SAMPLE FILES
Command Line Options

• Layout Simulation Options
  • `layout_netlist <path to netlist>`
    • Use to run sim on an existing layout extracted netlist
  • `noCaps`
    • Extract netlist with no capacitors
  • `noRes`
    • Extract netlist with no resistors

• If required files are not set up in run dir use:
  • `cdslib <path>`
  • `cell_list <path>`
  • `eldo_opt_file <path>`
  • `include_list <path>`
  • `readout_pins <path>`
  • `pin_bias_list <path>`
Command Line Execution

To be able to execute the script follow these steps:

1. Set up Required files in simulation directory
2. Make current working directory the simulation directory
3. Enter `run_eldo_on_cell.rb`
   - Include which ever options you have chosen

Example:

```
run_eldo_on_cell.rb --no_layout --FFT
```
Results Directory

• Location
  • When Eldo is finished running it will report back the location of results.
    • Ex:
      Eldo Finished, results can be found in
      /home/hmn/WA/c8_etest/hspice/c8Et/c8Et_MD510
      2_b/schematic_sim_tt_30C_trtc

• run_eldo_on_cell.rb stores simulation results
  in: /home/<usr>/WA/<DDC>/hspice/<library>/</cell>/
Results Directory

• **Generated files**- By `run_eldo_on_cell.rb`
  
  • `eldo.replay`
    • Contains command to launch eldo if changes are made to `.cir` file
  
  • `eldo.log`
    • Contains information regarding the execution of `run_eldo_on_cell.rb`
    • Options Used, launch directory, paths to input files
  
  • `results.csv`
    • CSV file of all read out pin data extracted from `netlist.chi`
  
  • `schematic_ext.nl`
    • Schematic netlist
  
  • `layout_ext.nl`
    • Layout Extracted netlist
  
  • `<cell name>.cir`
    • Circuit file used to launch eldo with all simulation settings compiled by `run_eldo_on_cell.rb`
Results Directory

• Generated files- By Eldo
  • `<cell name>.chi`
    • Results file for simulation
    • Read out pin out data is between a line that starts with X and line that starts with Y
  • `<cell name>.sw0*` (DC sweep only)
    • Binary file containing data/waveforms from DC simulation
  • `<cell name>.tr0*` (Transient sim only)
    • Binary file containing data/waveforms from transient simulation
  • `<cell name>.ac0*` (with use of `-FFT`)
    • Binary file containing data from FFT analysis

(*) Files can be viewed using `wavemaster`
Results Directory

• Ways to View Results
  • View binary files using wavemaster
  • Import results.csv into excel
  • Copy raw data from <cell name>.chi file
Appendix A: Sample Files

• Outline:
  • Required Files
    • inc_list
    • eldo_opt_file
    • bias_list
    • cell_list
    • readout_pins
  • Optional Files
    • RC_load
    • netlist_par
Appendix A: Required Files

- inc_list
  - [IC] and [PC] get substituted with the interconnect value and process corner value specified in the cell list. This enables multiple corner simulations for one cell
Appendix A: Required Files

- **eldo_opt_file**
  - Contains basic eldo simulation settings used for every simulation
Appendix A: Required Files

- **bias_list**
  - **Format**
    - `<pin>,<voltage>`

<table>
<thead>
<tr>
<th>Analysis</th>
<th>Replace <code>&lt;voltage&gt;</code> with</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Value</td>
<td><code>&lt;value&gt;</code></td>
</tr>
<tr>
<td>DC Sweep</td>
<td><code>swp,&lt;Vstart&gt;,&lt;Vstop&gt;,&lt;Vstep&gt;</code></td>
</tr>
<tr>
<td>Transient</td>
<td><code>pulse(&lt;V1&gt;&lt;V2&gt;&lt;Tdelay&gt;&lt;RiseT&gt;&lt;FallT&gt;&lt;PulseW&gt;&lt;Period&gt;)&lt;Tprint&gt;,&lt;Tstop&gt;)</code></td>
</tr>
</tbody>
</table>
Appendix A: Required Files

- **cell_list**
  - **Format**
    - `<Library>,<Cell>,<PC>,<Temperature_C>,<IC>`

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Values</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;PC&gt;</code></td>
<td><code>tt, ff, ss, sf, fs</code></td>
</tr>
<tr>
<td><code>&lt;IC&gt;</code></td>
<td><code>trtc, hrlc, lrc</code></td>
</tr>
</tbody>
</table>
Appendix A: Required Files

- **readout_pins**
  - **Format**
    - `<v or i>, <pin name>`

<table>
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<tr>
<th>Parameter</th>
<th>Typical Values</th>
</tr>
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<tr>
<td><code>&lt;v or i&gt;</code></td>
<td><code>v, i</code></td>
</tr>
</tbody>
</table>
Appendix A: Optional Files

- **RC_load**
  - **Format**
    - `<Pin1>,<Pin2>,<Resistor value>, <Capacitor value>`

- **netlist_par**
  - **Format**
    - `<Parameter>,<Value>`