EE 584: Introduction to VLSI

Project Report

ET Ring Oscillator – NAND

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1. Introduction

In the present work we have designed and tested a ring oscillator circuit using NAND gates. The ring oscillator was designed to fit inside the ETEST floor plan and outputs a signal with a certain frequency. An ETEST plan is nothing but a metal pad that is used for testing dies on a wafer for reliability and functionality. The frequency of the output signal obtained from the ring oscillator was set such that it is measurable by a standard 100MHz oscilloscope. All the design work was done using Cadence tools and the circuit was simulated using Spectre. Through this project we aim to measure the output signal frequency under different processing conditions.

2. Block diagram of the Circuit

The complete block diagram of the final circuit is shown in Error! Reference source not found. In addition to the core ring oscillator, it also consists of an enable circuitry to control the working of the oscillator, an output buffer to drive the load and a divider circuit to divide the raw output frequency of the oscillator by some factor. Error! Reference source not found. shows a symbolic pin diagram of the circuit. In total 5 pins were used, for providing $V_{dd}$, common ground, enable control and outputting the raw frequency and the divided frequency. A detailed description of the various blocks of the circuit is given below.

![Block diagram of circuit](image1.png)

Figure 1: Block diagram of circuit

![Pin diagram of circuit](image2.png)

Figure 2: Pin diagram of circuit
3. Ring Oscillator

3.1 Basics of Ring Oscillator

A ring oscillator is a device made up of several stages of an inverter, NAND or NOR gate. The individual units are connected in a chain and the output of the last unit is fed back to the first unit. If there are odd number of units, it can be shown that the output of the last unit will always be the logical NOT of the input to the first unit. If there are even numbers of units connected in series, the last output in this case is the same as the input. Hence, an even number of cascaded inverters with feedback can be used as a buffer. For the configuration with odd number of stages, the positive feedback of the output to the input causes the oscillator to oscillate. The oscillation frequency is given by,

$$f_{osc} = \frac{1}{n(t_{PHL} + t_{PLH})}$$

Where,

- $f_{osc}$ = frequency of oscillation
- $n$ = number of stages
- $t_{PHL}$ = delay time for output to change from high to low
- $t_{PLH}$ = delay time for output to change from low to high

A basic ring oscillator is shown in the fig[3].

A ring oscillator being self starting is used to test the speed of a process run and is often added to the test portion of a wafer. It is also used to measure the parasitic capacitance that often builds up within layouts. Another not very significant application of ring oscillators is to generate the clock frequency.

The oscillation frequency depends on the time delay in inverting the initial input and propagating the signal around the ring. The delay occurs due to the time taken by the transistor gate capacitance to charge before current can flow from source to drain. Thus the output of every unit changes after a certain amount of time after the input has changed. As the number of stages increase the total delay increases and hence the output frequency decreases. When all the individual units are made up of identical circuits, the delay due to one unit can be calculated by dividing the total delay with the number of stages.
3.2 Enable Circuit for the ring oscillator

The enable circuit provides the user a way to control the operation of the ring oscillator. When the user provides logic one on the enable pin, the ring oscillator operates and generates sustained oscillations. When the enable circuit input is logic zero no oscillations are generated by the ring oscillator.

To design the enable circuit, we have made use of the NAND gate already incorporated as one of the stages of the oscillator. From the truth table of the NAND gate, it can be seen that when one input of the NAND gate is at logic high, the output of the NAND gate is always the logical NOT of the second input. For instance if we call the NAND gate inputs as ‘A’ and ‘B’ and the output as ‘\( \Theta \)’, and A is set to be logic high all the time, then if \( B = 0 \), \( \Theta = 1 \) and if \( B = 1 \), \( \Theta = 0 \). In short the NAND gate act as an inverter with one input perpetually set to high. As against this, when one of the inputs is always set to logic low, then the output of the NAND gate is always logic high. Symbolically if A is set to zero, then if \( B = 0 \), \( \Theta = 1 \) and if \( B = 1 \), \( \Theta = 1 \).

Using this argument the first oscillator NAND gate stage can be used as enable circuit table 1. When the enable is at logic high, this NAND gate will act as an inverter, and thus we have odd number of cascaded NOT gate stages to generate sustained oscillations. When the enable input is at logic low, then the NAND gate output will always be one followed by even number of NOT gate stages, which will just act as a buffer and hence there will be no oscillations.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1 Truth table of NAND gate

3.2.1 Schematic and Layout

Cadence layout and schematics for the NAND gate configuration used as enable circuit are shown in figures [4] and [5]. The NMOS and the PMOS devices were designed with width 5.
3.3 Core Ring Oscillator

The core ring of the oscillator was designed to have 85 NAND gate stages. To determine the total number of NAND stages, a 5 stage ring oscillator was first simulated. The total delay was found to be 3.28 ns. This gives the individual delay of a single NAND gate stage to be about
0.6 ns. In order to see the output on a 100MHz oscilloscope, the output frequency of the final circuit was tentatively fixed to be 20MHz accordingly simulations were done by adding the inverter stages step by step. The 5 stages was first extended to twenty stages, then fifty stages and subsequently to 85 stages. The total delay after 85 stages was found to be 52ns which is approximately, 19.2MHz.

3.3.1 Schematic and Layout

The NAND gate stages used in the ring, were used in the configuration where both the inputs are shorted. This configuration has an advantage over the other one which was used for the enable circuit, in that it helps in reducing the layout area. In the second configuration, we need to connect one input to Vdd always. This amounts to increase in the metal routings which make laying out the circuit difficult and increases the area.

The schematic and layout of a single NAND gate stage used in the ring oscillator is shown in the figures [6] and [7]. The widths of the CMOS devices were experimentally determined to be 5. This width was selected by trying out different combinations on a 5 stage ring oscillator circuit and it was observed that the delay is minimum for $W_P=5$ and $W_N=5$. The observations for different combinations of widths are shown in table…. (note: need to be inserted)

![Figure 6: Schematic of one stage inverter built with NAND gate](image-url)
3.3.2 Schematic and Layout of 85 stage Ring oscillator circuit
The schematic and layout of 85 stage Ring oscillator circuit is shown in fig[8] and fig[9].
3.3.3 Simulation Result

The simulation result of the 85 stage RO is shown in figure[10]. The delay was found to be 51.0409ns that is a frequency of 19.5MHz.
4. Output Buffer

One of the common applications of the ring oscillator is to generate a clock which drives a subsequent circuit. The capacitance of the subsequent circuit acts as load to the ring oscillator and hence the ring oscillator should have the capability to drive this load.

This project was designed to work with a 100MHz oscilloscope which typically has a 10pF input capacitance. In order to make sure that the circuit works with 10pF load, the ring oscillator was simulated with one. It was observed that the ring oscillator alone was not capable of driving the load. So an output buffer was introduced in the proposed circuit and cascaded with the ring oscillator.

The output buffer is ideally an inverter or a chain of inverters. The width of the PMOS and NMOS of the inverter and the number of inverter stages in the output buffer is decided based on the load. To determine the number of inverter stages to be used in the buffer, experiments were done using different CMOS device widths and number of stages. Other things that were considered while designing the output buffer circuit were less number of stages as increasing the number of stages further increases the delay and minimum layout area. Also the requirements of about 50ns of time period of the output signal had to be considered.

Under all the above considerations and experiments, a five stage output buffer with PMOS / NMOS width as 5/3 was found to be the most viable option. The widths of the PMOS and NMOS were chosen such that they had equal rise and fall times. The 5/3 width of the inverter was chosen instead of the minimum width considering the area occupied of the output buffer and having minimum number of stages. Experiments were also done to determine the number of stages. The results of simulating the ring oscillator with different number of output buffer stages are as shown in table[2].

<table>
<thead>
<tr>
<th>Number of stages</th>
<th>Rise time</th>
<th>Fall time</th>
<th>Time period</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four stage (Multiplication factor of 27)</td>
<td>15.1ns</td>
<td>14.02ns</td>
<td>52.47ns</td>
</tr>
<tr>
<td>Five stage (Multiplication factor of 81)</td>
<td>4.9ns</td>
<td>5.0ns</td>
<td>52.47ns</td>
</tr>
<tr>
<td>Six stage (Multiplication factor of 243)</td>
<td>1.2ns</td>
<td>1.2ns</td>
<td>52.47ns</td>
</tr>
</tbody>
</table>

Table 2: The observations of different stages for an output buffer

The five stage output buffer was preferred over the four stage one as it is able to charge and discharge the capacitor fully and has a considerable low rise and fall time. When compared to six stage output buffer, it occupies less area and also there is not much difference in the rise and fall time.

All the five stages were connected in series with each other. The widths of the PMOS and NMOS in the cascaded inverters were incremented by a factor of three at each stage to drive the capacitive load effectively. Folding techniques were used while laying out the PMOS and NMOS transistors in parallel to effectively decrease the total area occupied in the chip. The schematic and layout of the first stage of the inverter is shown in the figures [11] and [12].
Figures[13] and [14] show the schematic and layout of the second stage of the output buffer that uses a multiplication factor of 3.
The schematic and layout of the final Output buffer having 5 stages of the inverters is shown in the figures[15] and [16].
4.1 Schematic, layout and simulation results

Figure 15: Schematic of the Output Buffer

Figure 16: Layout of the Output buffer
The simulation output of the output buffer when connected to the ring oscillator gives 52.47ns of the time period which is closer to the desired time period of 50ns. Figure [17] shows the simulation output result.

![Simulation output result](image)

**Figure 17: Simulation output of the output buffer**

### 5. Divider Circuit

A cascade of D flip-flops is used for implementing the divider circuit. The divider circuit divides the frequency of the output obtained from the output buffer by a factor of 1024. A single D flip-flop divides the frequency of the input signal by two. So in order to reduce the frequency by the desired amount, a cascade of 10 D flip-flops is used in the circuit.

#### 5.1 D Flip-flop:

A D flip-flop is a logical device that has two stable states. The output of a D flip-flop always follows the input signal and changes the state only when a control signal or the clock signal is activated. For this project a positive edge triggered D flip-flop is used. A positive edge triggered flip-flop changes its state only when the clock transits from logic low to logic high. The flip-flop remains in that state till the next rising edge arrives at the clock input. A master slave D flip-flop consists of two D latches and is called so because the second latch changes its state only as a response to a change in the master latch’s state. A D flip-flop has two outputs, one is the desired state and the other is the complement of this output. When the complemented output is connected back to the clock, the flip-flop toggles at every output state and divides the input at D by two.

Figure[18] shows a basic D flip-flop circuit in master-slave configuration. It consists of transmission gates and inverters to latch the input. When the clock goes low, transmission gates
T1 and T4 are on. The D input is passed by T1 and the inverted input is stored at point B. Since T3 is off, the input is not passed to the second latch. Also since T2 is off, the output of the first latch feedback loop does not interfere with the input. Whatever was the previous output at Q, is latched by the second latch and as T4 is on, the output at Q remains same. When a positive edge arrives at the clock, T1 and T 4 are turned off and T2 and T3 are turned on. Due to T2, the input at D keeps circulating in the

![Figure 13.22 An edge-triggered D-FF.](image)

Figure 18 Edge Triggered D-FF

first latch and hence the D input can now be removed. Now as T3 is on, the inverted input at B is passed on to the second latch, where it again gets inverted and is passed on to Q. When the clock again goes low, T1 and T4 are turned on and the same cycle repeats itself. Due to the master slave configurations, effect of noise that can lead to metastability can be avoided.

### 5.2 D Flip-flop Schematic

Figure [19] shows the schematic of a single D flip-flop stage which was designed using the cadence tool. The inverter blocks are instances of the inverter schematic shown in figure [20]. An important consideration that should be made while designing this circuit is the rising time of the clock. If the clock rise time is high, the transmission gates will not switch fast enough to latch the input. This may lead the flip-flop into an undesirable metastable state.
The transmission gates were designed using PMOS and NMOS devices with minimum width of 1.05µm. Similarly the CMOS devices used in the inverter were taken to be of width 1.05µm.

Figure 19: Schematic of single stage D-flip flop

Figure 20: Schematic of inverter used for D-flip flop
5.3 D Flip-flop Layout

The D flip-flop layout as laid in the cadence tool is shown in figure[22]. The top level layer used is the metal 1 layer. The interconnections are done using either poly layer or the local interconnect (LI) layer. The layout passed the DRC, CLDRC, as well as the LVS tests without any errors. The inverter layouts were instantiated and the individual inverter layout is as shown in figure [21].
Each flip-flop divides the input frequency by two. So if we have \( n \) flip-flops connected in series, the output frequency will be reduced by \( 2^n \). In this project, 10 D flip-flop stages were used to reduce the output frequency by \( 2^{10} = 1024 \). The schematic and layout of the cascaded D flip-flop stages is as shown in figures [23] and [24].
6 The Final Circuit Schematic and Layout

The layout and schematic of the circuit with ring oscillator, enable circuit, output buffer, D flip-flop is shown in figures[25] and [26].
Figure 26 Layout consisting of enable, 85 stage ring oscillator, output buffer, 10 stage D flip flop.

Figure [27] below shows the simulation result of simulating the entire circuit under typical conditions. The total delay is observed to be about 67 ns.
7 E-Test Pad:
The E-test pad of size 100μm x 100 μm is shown in the layout below.

![Figure 28: E-Test pad](image)

The ET floor plan consists of 12 test pads of size 100μm x 100μm and spaced by an interval of 125μm. Five out of twelve pads were used which serve as input or output pins and are named raw output, divided output, V\(_{dd}\) for ring, common ground, V\(_{dd}\) for buffer and enable signal. The ‘raw’ output is the output straight out of the output buffer. The ‘divided’ output is from the divider circuit. The ‘V\(_{dd}\)’ pad provides supply voltage (1.8 Volts) to the ring excluding the buffers. The ‘V\(_{ddbuffer}\)’ pad provides the supply voltage for the buffer. The ‘enable’ signal acts as a switch to either turn the circuit on (ring oscillates) or switch it off (ring oscillator doesn’t oscillate). Figure [29] shows the circuit laid out in the ET floor plan and the corresponding pins routed to the bond pads. (Still to be done).

![Figure 29 Layout of complete circuit in the bounding box](image)
8 Design Considerations

The main aim while designing a circuit is that the fabricated circuit performs satisfactorily under different operating conditions and parameter involved in the design. In general there are three different sources of variation – two environmental and one manufacturing. These are process variations, supply voltage, and operating temperature.

8.1 Process Variations

The variations in certain parameters that bring about significant changes in the performance of a device are known as process variations. There are three types of process variations:

- Lot to lot (inter process variation)
- Wafer to wafer (inter process variation)
- Die to die (intra process variation)

A distribution is shown in the Figure[30] which has standard deviation as its x-axis and count as the y-axis. The distribution is plotted to see the effect of different physical parameters, for example, in case of interconnect we take poly line width, spacing, oxide thickness ($T_{ox}$), doping, contact resistances etc.

![Process variation](image)

Figure 30: Process variation
A plot of standard deviation (of the physical parameter) versus count is done. The devices which lie within +/-3σ deviation are only accepted. This way percentage of failure of the parts is reduced to 0.26%. Therefore attempts are made to artificially limit the distribution so as to reduce the failure rate to the minimum possible value. The Figure 1 gives a pictorial representation of the 6-σ process.

8.1.1 Variation in Power Supply

The Power Supply given to a circuit is the electrical parameter associated with the design. The Vdd given to the circuit may vary over a certain range. Hence the circuit is tested for a +/-5% change in Vdd. The change in the Vdd influences the ‘I_{ds}’ and hence a change in delay is observed. The delay is less for high voltages and high for low voltages.

8.1.2 Variation in Temperature

The ambient temperature at which a circuit operates is the environmental parameter associated with the design. This varies widely even under normal conditions. Therefore it is extremely important to test whether the circuit provides a satisfactory performance for a wide temperature range which is taken as -40°C to 125°C. The typical temperature is 27°C.

The ‘I_{dsSat}’ of a device depends upon mobility and V_{th}. Both mobility and V_{th} vary inversely with temperature. Since ‘I_{dsSat}’ is proportional to \((V_{gs}-V_{th})^2\) at low V_{gs}, V_{th} dominates and current increases with increase in temperature. At high V_{gs}, mobility dominates and therefore current decreases with increase in temperature.

8.1.3 Design Corners

In CMOS, there are two types of transistors with somewhat independent characteristics, so the speed of each can be characterized. The term corner refers to an imaginary box that surrounds a guaranteed performance of the circuits. A design corner constitutes of various parameters all of which are set to extreme limits. Some of the corners may hardly exist in reality like fast-slow and slow-fast and are called skew corners. Simulation of such corners is not performed in our design.

8.1.4 Transistor Corners

When the parameters of a transistor are set in such a way that the transistor operates fast then it is known as a fast corner. The V_{th} is set to a much lower value and the T_{ox} is also decreased in comparison to the typical parameters in case of an Nmos. Thus there is increase in I_{ds} and the transistor operates faster. Similarly the parameters are modified in vice versa manner for the slow corner.
8.2 Simulations for comparison of corners

To decide whether the circuit designed is suitable for varying parameters it is simulated over a wide range of device parameters, input parameters. The plots obtained are used to determine the performance. The figures….. show the raw output of the ring oscillator for three corners of typical, fast and slow respectively at vdd=1.8v and typical temperature. The effect of the enable signal is also seen here.(Note: Figures are to be inserted.)

Fig2 : simulations for Fast process corner at temp=27°c and vdd =1.8v with enable signal

Fig3 : simulations for Typical process corner at temp=27°c and vdd =1.8v with enable signal

Fig4 : simulations for Slow process corner at temp=27°c and vdd =1.8v with enable signal

Two Line plots are drawn from the various simulations performed for different combinations of corners, Vdd and temperatures. All the values for simulations are shown below in Tabular form at the end of the document.

![Deviation of different corners w.r.t to Typi at vdd =1.8v](Image)

Figure 31:Delay Vs Temperature for different process corners at Vdd=1.8v
Deviation of different corners w.r.t to Typi at nominal temperature 27deg

<table>
<thead>
<tr>
<th>Vdd (v)</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.62</td>
<td>250</td>
</tr>
<tr>
<td>1.8</td>
<td>200</td>
</tr>
<tr>
<td>1.98</td>
<td>150</td>
</tr>
</tbody>
</table>

Figure 32: Delay Vs Temperature for different process corners at Nominal temperature

Three surface plots are drawn from the various simulations performed for different combinations of corners, Vdd and temperatures. All the values for simulations are shown below in Tabular form at the end of the document.

Fast - Fast

Figure 33: 3D surface plot for Fast –Fast process corner
Figure 34: 3D surface plot for Typi –Typi process corner

Figure 35: 3D surface plot for Slow -Slow process corner
8.3 Observations

1) Raw frequency measurement under different corners:-
   It was observed that the range of frequency variation obtained when complete circuit is in
   place at typical temp of 27° C and vdd 1.8v are
   a) 30.3 - 40.46MHz for Fast-Fast process corner.
   b) 10 – 21.3MHz for Typi - Typi process corner.
   c) 3.76 – 15.9MHz for Slow -Slow process corner.

   All other values are tabulated below in Table III.

1) Delay varies inversely with Vdd. This justifies the fact that speed varies almost proportional to
   Vdd. Larger the Vdd lesser the delay and vice-versa. It varies proportionally with the corners. It
   is large for slow corners and less for fast corners.

2) Delay varies inversely with temperature. It is low for high temperatures and high for low
   temperatures. The increase in W/L results in larger I_{ds} and hence faster operation and thus lesser
   delay. Therefore by increasing the size it is observed that delay is reduced significantly.

Corners which are generally used:
1) Fast transistor corner: highest Vdd and lowest temperature
   This corner is the fastest one and it has the minimum delay. This configuration used when we
   need high speed circuits where high power dissipation can be tolerated.

2) Slow transistor corner: lowest Vdd and highest temperature
   This corner is the slowest one and it has the maximum delay. This configuration is used when we
   need to implement circuits with very low power dissipation.

\[
\begin{array}{|c|c|c|c|c|c|c|c|}
\hline
\text{Vdd =1.8v} & -40 & 0 & 27 & 80 & 125 \\
\hline
\text{Typi-Typi} & 100.082 & 72.826 & 65.431 & 54.2646 & 46.73 \\
\text{Slow-Slow} & 265.92 & 213.45 & 167.018 & 117.346 & 62.838 \\
\hline
\end{array}
\]

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Temperature =27celcius} & 1.62 & 1.8 & 1.98 \\
\hline
\text{Typi-Typi} & 106.69 & 67.431 & 40.73 \\
\text{Slow-Slow} & 260.17 & 167.018 & 78.203 \\
\hline
\end{array}
\]

Table 3 :2D Plot Values Tabulated for different corners
Table 4: 3D Plot Values Tabulated for different corners

These tabular values calculated with temperature range of -40°C to 125°C

Fast – Fast Process corner

<table>
<thead>
<tr>
<th>Vdd(v)</th>
<th>Frequency Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.62</td>
<td>15.3 – 32.5</td>
</tr>
<tr>
<td>1.8</td>
<td>30.3 - 46.26</td>
</tr>
<tr>
<td>1.98</td>
<td>48.06 – 60.69</td>
</tr>
</tbody>
</table>

Typi – Typi Process corner

<table>
<thead>
<tr>
<th>Vdd(v)</th>
<th>Frequency Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.62</td>
<td>6.2 – 13.4</td>
</tr>
<tr>
<td>1.8</td>
<td>10 – 21.3</td>
</tr>
<tr>
<td>1.98</td>
<td>19.9 – 30.25</td>
</tr>
</tbody>
</table>

Slow – Slow Process corner

<table>
<thead>
<tr>
<th>Vdd(v)</th>
<th>Frequency Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.62</td>
<td>1.2 – 5.79</td>
</tr>
<tr>
<td>1.8</td>
<td>3.76 – 15.9</td>
</tr>
<tr>
<td>1.98</td>
<td>6.74 – 14.9</td>
</tr>
</tbody>
</table>

Table 5 frequency values for different corners
9. References:
2. www.wikipedia.org
4. Lecture notes by Dr Joseph Elias http://www.engr.uky.edu/~elias/index_584.html.