Class 13: Flip Flops

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Class 13: Flip Flops
Introduction (Martin c.7)

Flip Flops basics:
• Storage elements for synchronous circuits (what is synchronous?)
• Break up any race conditions or oscillations, i.e., feedback loops around a cyclic logic circuit
• Inputs: normally have 1 or 2 input signals and a clock
• Outputs: differential outputs Q and Q’
  • output latched or stored on rising/falling edge of clock
  • output stable until next rising/falling edge of clock
• Can optionally have set and/or reset asynchronous inputs
  • regardless of state of the clock, the outputs will either be set to a 1 or reset to a 0
• Typical techniques
  • master_slave
  • edge_sensitive
• Typical configurations:
  • SR (set_reset)
  • D
  • JK
  • T (toggle)
• D FF is the most common for ICs

SR flip flop symbol
• changes on positive going clock edge

SR flip flop symbol
• changes on negative going clock edge
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Types of Flip Flops (Martin c.7)

• D

<table>
<thead>
<tr>
<th>D</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

• SR

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q_n</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Indeterminate</td>
</tr>
</tbody>
</table>

• JK

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q_n</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Q_n</td>
</tr>
</tbody>
</table>

• T

<table>
<thead>
<tr>
<th>T</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Q_{n+1}</td>
</tr>
<tr>
<td>1</td>
<td>Q_{n+1}</td>
</tr>
</tbody>
</table>

realized by tying J and K together from a JK FF
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Types of Flip Flops (Martin c.7)

• D
  • cascade of two latches with opposite clock phases
  • best choice (usually) for IC design
  • after FF is clocked, output is equal to the D value just before the clock changed

• SR
  • same as D FF if S=D and R=D’
  • can be set, reset, or remain in its previous state
  • indeterminate state exists if S=R=high when CLK=low
  • major limitation is output can be affected by the input at any time the CLK is high, a.k.a., noise problem

• JK
  • often used for synchronous machines or counters
  • J=1, K=0    FF is set
  • J=0, K=1    FF is reset
  • J=0, K=0    No change
  • J=1, K=1    FF state toggles (difference between JK and SR, but same noise limitation)

• T
  • useful in counters
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D Flip Flop Operation (Martin c.7)

Clk is ‘1’, implies master active, slave latched
B=D=1 since 1 or anything is 1 in ‘c’

Clk is ‘1’, implies master active, slave latched
B=D=0 since 1 or anything is 1 in ‘d’

Clk=0

Clk is ‘0’, implies master latched, slave active
Q’=D’=0 since 1 or anything is 1 in ‘h’

D=0

Clk is ‘0’, implies master latched, slave active
Q’=D’=0 since master disabled by ‘a’ and ‘b’
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D Flip Flop Master Circuit (Martin c.7)

Figure 7.17 The logic diagram of a master–slave D flip-flop.

[Diagram of D Flip Flop Master Circuit]

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D Flip Flop Circuit (Martin c.7)

\[ S = 1 : Q = 0 \text{ immediately, } Q' = S' \text{ after inv delay} \]
\[ R = 1 : Q' = 1 \text{ immediately, } Q = R' \text{ after inv delay} \]
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Tristate Inverter (Weste c.2)

- Cascade of a transmission gate with an inverter
- C=0 → C=1: Z is tristated, i.e., A does not influence Z
- C=1 → C=0: Z = A'
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Flip Flop Ideas (Martin c.7)

- Biphase D FF
- asynchronous Set and Reset
- Inverter Based

- Biphase D FF
- transmission gates used
- NOR based

Figure 7.27 A transmission-gate-based master–slave D flip-flop.
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Flip Flop Ideas (Martin c.7)

- Biphase JK FF
  - transmission gates used
  - Inverter based

Design Assignment
- Biphase D FF (clk, clk’)
- buffer the D input with a tristate inverter
- Inverter based
- Asynchronous Reset
- hint: can optimize the layout by rearranging ckt