Class 11: Transmission Gates, Latches

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4. X-Gate XOR
5. X-Gate 8-to-1 MUX
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9. n-CH Pass Transistors vs. CMOS X-Gates
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Transmission Gates (Martin, c5.1)

• Pass Transistors, a.k.a., Transmission Gates are same as a relay
• Why? Usually allows for a reduction in number of transistors

NMOS

\[ \begin{align*}
\text{Vcntl} & : H & \text{L} \\
\text{Out} & : Z & \text{In}
\end{align*} \]

CMOS

\[ \begin{align*}
\text{Vcntl'} & : L & \text{H} \\
\text{Out} & : Z & \text{In}
\end{align*} \]
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Transmission Gate 2-to-1 MUX (Martin, c5.1)

This same design will be revisited shortly for an 8-to-1 MUX
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Transmission Gate XOR (Martin, c5.1)

- XOR similar to 2-to-1 MUX
- NMOS version:

<table>
<thead>
<tr>
<th>B</th>
<th>A</th>
<th>Q1(n)</th>
<th>Q2(n)</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>off</td>
<td>on</td>
<td>0 (A)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>on</td>
<td>off</td>
<td>1 (A')</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>on</td>
<td>off</td>
<td>0 (A')</td>
</tr>
</tbody>
</table>

- CMOS version:

**Table 5.1 The Truth Table of the exclusive-or Function**

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>pseudo-NMOS</th>
<th>CMOS</th>
<th>CMOS</th>
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</thead>
<tbody>
<tr>
<td>X-Gate</td>
<td>6</td>
<td>traditional</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>X-Gate</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Transmission Gate 8-to-1 MUX (Martin, c5.1)

Typically, one would not use more than 8-to-1 MUX. Why?
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Transmission Gate Clocked Latch (Martin, c5.1)

When CLK is high:

\[ V_{\text{in}'} \]

“track mode”, latch is loaded

When CLK is low:

\[ V_{\text{in}} \]

\[ V_{\text{in}'} \]

data is latched to \( V_{\text{in}} \) at time of clock transition
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Voltage Drop of n-CH X-Gates (Martin, c5.1)

Desired operation:
• Start with $\phi_{\text{clk}} = 1$, $V_{G2} = V_{\text{in}}$
• Transition, $\phi_{\text{clk}} 1->0$, Q1 on->off, $C_p$ keeps voltage
• AKA source follower or common drain buffer
• $C_p$ is due to what?
• $V_{\text{out}} = V_{\text{in}}’$

Problems with circuit:
• Start with $V_{\text{in}}=0$, and $\phi_{\text{clk}} 0->1$
• $V_{G2} = V_{\text{in}} = 0V$, so Q1 S/D are at ground (Q1 is in what region?)
• If $V_{\text{in}} -> V_{\text{DD}}$, while $\phi_{\text{clk}} = 1$, initially LHS of Q1 is drain RHS is the source, and $V_{gs}=V_{\text{DD}}$, and $V_{gd}=0$
  (Q1 is in what region?)
• $V_{G2}$ charges up to $V_{\text{DD}}-V_{tn}$
• $V_{\text{eff}}$ for Q1 will become zero ($V_{gs}-V_{tn}=0$)
• Q1 shuts off when $V_{gs}=V_{tn}$, or when $V_{G2} = V_{\text{DD}}-V_{tn}$
• Thus $V_{G2}$ never gets to $V_{\text{DD}}$, and body effect determines how far from $V\text{DD}$ the node ends up
• As body effect goes up, $V_{tn}$ goes up, $V_{G2}$ goes down
• So what is the problem?
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Voltage Drop of n-CH X-Gates (Martin, c5.1)

Through how many series transistors does the data pass?

- Equivalency says that two series transistors with W/L is the same as one transistor with W/2L

- Voltage at gate of Q3 is the same, it just takes longer to rise

=>

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n-CH vs. CMOS X-Gates (Martin, c5.1)

- Area may be smaller if NMOS used vs. CMOS
- CMOS X-Gates transfer “1” and “0” efficiently. Why?
- CMOS X-Gates after faster in 0->1 transition. Why?
- N-CH voltage drop a major disadvantage, but can be eliminated

Speed:
- When junction capacitance dominates, which should be used?
- When load capacitance dominates, which should be used?

Power:
- Which is more sensitive to Vt value?
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Full-Swing n-CH X-Gates (Martin, c5.1)

• Applicable when an inverter follows a pass transistor

• Q4 must have W/L small compared to Q1 for 1->0 at Q2 gate. Why?

• p-ch load (Q3) will be completely turned off with the addition of Q4. If not, what would occur?
• What happens to voltages when $\phi_{\text{clk}}$ is high and $V_{\text{in}}=1$?

• $C_p$ obtains what value?

• What happens to $C_p$ if $\phi_{\text{clk}}$ remains low?

• How does this vary with temperature?

• What else would cause this to vary?
Example of a two cross coupled inverters, having positive feedback:

Latch realized below using what type of logic?
What has changed from previous slide for latch?

When CLK is high, D is passed to V1, but why is it not inverted by Q5/Q6?

Good: hysteresis is added, noise immunity for slow-moving signals, less area than latch of previous foil

Bad: Only inverter a is a driver. Why?
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Static CMOS Digital Latches (Martin, c7.1)

• Q1 is used as a pass transistor, so why is Q2 in the circuit?

• Q2 ratio W/L should be small or large compared to Q1?

• When CLK is low, Q3 is on, reinforcing a stored “0” at V1.

• What reinforces the stored “1” at V1 when CLK is low?
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Static CMOS Digital Latches (Martin, c7.1)

- Cross coupled NOR gates
- $Q = D$ when $Clk = 1$
- $Q$ preserved when $Clk = 0$

- As $CLK \ 0 \rightarrow 1$, $Q' \rightarrow gnd$ if $Q_5/Q_7$ widths are larger than $Q_3$
- $Q_5$ series with $Q_7$ gives what width?
- Compare to what width of $Q_3$?
- When $Q'$ is low, $Q_4$ is on, $Q_2$ off, $Q$ is 1
- This means one inverter delay