

Design Project 3

Project Overview

The most typical form of operational amplifier is called a two-stage opamp and consists of an input differential stage and a second high-gain stage. This project deals with the design of differential amplifier that could be used as the input stage of a two-stage opamp.

Due Date

The official due date for Design Project 3 is Tuesday, Nov. 28. However, since the Final Design Project is due only one week later, I suggest you try to get this done as soon as possible.

Groups

You are to design one circuit according to the specifications below. This project may be done as entire 3-4 person groups or as individuals if you do not have time to work with your group.

What to Turn In

For Design Project 3 you should not write a report, but you must submit the final circuit (in B²SPICE) as an email attachment to Dr. Mason (mason@engr.uky.edu). The submitted circuit should be ready to simulate and should generate a .OP and .AC analysis when the simulation is run. In the email message with your circuit attached, be sure to include the following information:

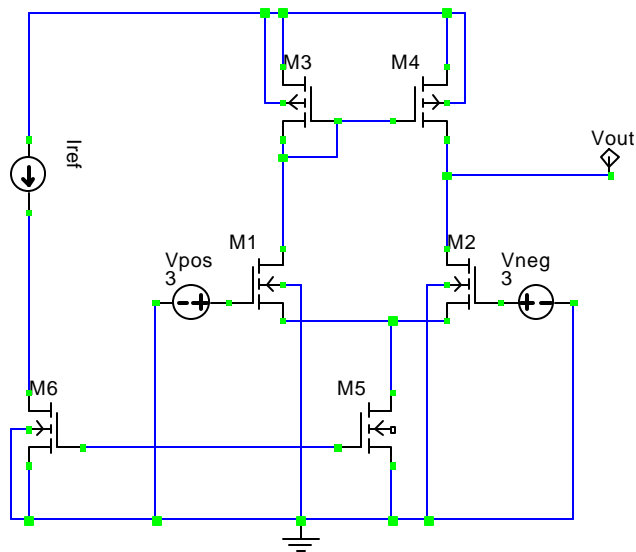
- Team Members: list of students who should receive a grade for the attached circuit
- SPICE Version: is the circuit done in B²Spice ver. 2, or in B²Spice 2000.
- Results: list the following results which will be verified by simulating your circuit
 - DC Gain (max gain at low frequency) in dB
 - -3dB Frequency
 - Output Voltage DC level
 - Total Power Consumption
 - Total Transistor Size (determined from formula below)

Background

Differential amps can have either an nMOS input, like the one shown below, or pMOS inputs. For reasons we will discuss in class, it is often preferred to use a pMOS-input differential amp, which is what you will do for this project. The circuit below is just for reference and should not be copied as in the previous two design projects. For this project, you will do all of the design without being given a starter circuit.

In this project, rather than design for gain and bandwidth goals, you are to maximize these to parameters within set limits on power consumption and transistor size. *Power consumption* can be calculated by multiplying the total current from the power supply ($I(VDD)$) by the power supply voltage. Here you are limited to 500 μ A of total current, or 3mW total power. For transistor size, you are limited to a maximum dimension of 300 μ m for any single transistor, for example, a transistor with $L=2\mu$ m and $W=300\mu$ m would be maximum size. Your netlist will be checked to ensure you follow this specification. In addition, you should estimate the total area of your circuit by calculating the total gate area of the transistors in your circuit. To do this, simply multiply $W \times L$ for each transistor and sum the results for all six transistors.

$$SIZE = W_1L_1 + W_2L_2 + \dots + W_6L_6$$



nMOS-input Differential Amplifier: Note, you must design a pMOS-input amplifier which will look like the compliment of this schematic.

To measure the gain of a differential amplifier you must set both inputs to an appropriate DC voltage (3V, in this design) and assign the positive input (Vpos, below) as the only AC source in your schematic. You can then measure the gain from the .AC analysis by looking at the output (Vout). Although in most cases you will get correct results if you simply plot the expression

$$\text{DB}(V(\text{out-node-number}))$$

it is suggested that you plot

$$\text{DB}(V(\text{out-node-number})/V(\text{in-node-number}))$$

Design Specifications

Design a pMOS differential amplifier which is the compliment of the nMOS version shown above. Your circuit should include the standard 5 transistors for the differential amplifier, an additional transistor to form a current mirror (like M6 above), a 5pF load capacitor, a reference current source, and a VDD power supply (not shown above).

You must also follow these guidelines:

- DC input voltage is 3V for both input transistors
- Apply an AC input to the positive input terminal only
- Output load capacitance is 5pF
- DC output voltage must be between 1.5 and 2 volts
- Total power consumption (see above) must be less than 3mW
- Maximum transistor dimension (W or L) is 300 μ m

Given these specification, you are to maximize the gain and -3dB frequency. As specified above, when you submit your circuit file by email, you should also provide a listing (within the body of the email message) the following data.

- DC Gain (max gain at low frequency) in dB
- -3dB Frequency
- Output Voltage DC level
- Total Power Consumption
- Total Transistor Size (determined from formula above)

Additional Information

In addition to the above specification, you should follow the guidelines below which have been used in Design Project 2:

- use the same Level 1 MOS model parameters which include capacitances
- use 4-terminal devices (like *mos_n_lv1l_4*) where appropriate
- use a minimum size of $W=5\mu\text{m}$ and $L=2\mu\text{m}$ with a resolution of $0.5\mu\text{m}$
- $V_{DD} = 6\text{V}$
- set source and drain areas and perimeters as in Design Project 2
- anything else that I may have forgotten

Be sure to check the orientation of pmos transistors. Although the source and drain terminals should be identical, I have noticed that 4-terminal devices will only work one way (i.e. if you flip source and drain it will not work correctly). To check this, look at the netlist which should show the transistor terminal nodes in this order (Drain Gate Source Substrate).