

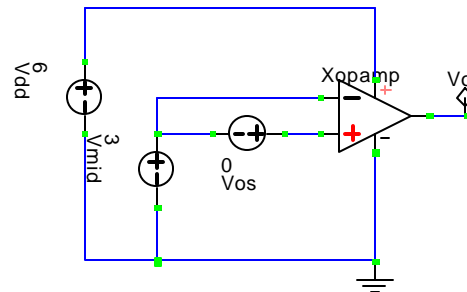
Solutions to Homework 10

These problems deal with determining the configurations necessary to simulate the op amp performance parameters as required in your design project. Since this homework is directly related to your design project, you may work on this assignment in your design groups, but each student should turn in the homework solution individually. To answer each of the following problems you should discuss what inputs are necessary, what SPICE analysis will be required (e.g. .AC or .DC), what outputs will be measured/plotted, and how the performance parameter will be measured. In addition, simulation of some parameters will require different configurations such as open loop analysis or unity gain feedback. For each problem, draw the required configuration using a block diagram op amp and show inputs for each configuration. Assume you have a voltage source called $V_{mid} = V_{DD}/2 = 3V$ which will be used as the input reference DC level rather than using a ground reference as would be done in a dual supply op amp. If there are any questions regarding this, be sure to ask about it in class.

Problem 1: Offset Voltage (5pts.)

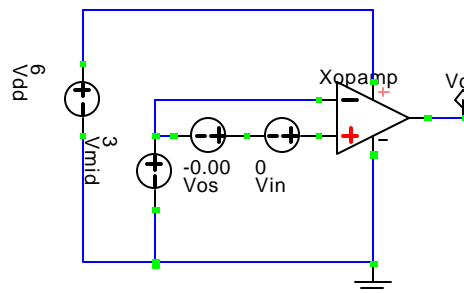
If there is offset error in an op amp, the output voltage will not be zero when both inputs are grounded. For our single-sided op amp, this would translate to the output voltage not equal to $V_{DD}/2 = 3V$ when the both inputs are set to $V_{DD}/2 = 3V$. The offset voltage is defined as the input voltage required to set the output to ground (or $V_{DD}/2$ in our case). Since several of the performance parameters can only be measured accurately if there is no offset voltage, the task in Problem 1 is to determine the output offset voltage so that it can be applied to the input in subsequent problems in order to nullify the offset. Describe how the offset can be measured.

- Open loop configuration shown on the right
- Negative input at V_{mid}
- Positive input at $V_{mid} + V_{os}$
- Perform a DC analysis to vary V_{os} over a small range in which V_o is near 3 V.
- Plot V_o vs. V_{os} and measure the input voltage at which $V_o = 3V$.
- The offset voltage will be $V_{offset} = -V_{os}(V_o=0)$ since it is the voltage required to make the output equal to zero.
- Verify by setting V_{os} to V_{offset} and checking the output voltage to insure it is 0V.

**Problem 2: DC Gain (10pts.)**

The DC gain of an op amp describes how much the output voltage changes relative to an input voltage change. The DC gain will be very similar to the low frequency small signal gain as found in several previous homework problems. However, for this design project, you should measure the DC gain by plotting the output voltage vs. input voltage over a very small range of input in which the output swings from its maximum to its minimum. The measurement should also provide any necessary correction for offset voltage error. Describe how to measure the DC gain of the op amp.

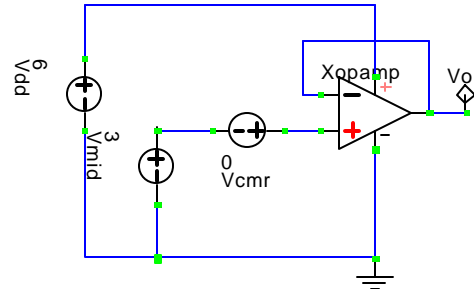
- Open loop configuration shown on the right
- Negative input at V_{mid}
- Positive input at $V_{mid} + V_{os} + V_{in}$
- Perform a DC analysis to vary V_{in} over a small range in which V_o goes from minimum to maximum.
- Plot V_o vs. V_{in} and measure the slope (V_o/V_{in}) where the op amp is amplifying (i.e. where V_o increases with V_{in})
- The DC gain is the slope of V_o vs. V_{in}



Problem 3: Common Mode Input Range (10pts.)

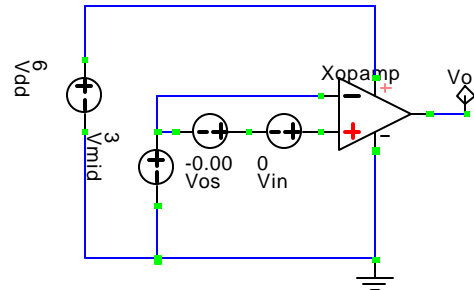
In a unity gain feedback configuration the output is tied to the inverting (negative) input, and the output will follow the DC level of the input (applied to the positive input). In this configuration, the output will follow the input over an input voltage range called the Common Mode Range (CMR). When the input is above or below the CMR, the output will no longer directly follow the input. The CMR represents the useful DC input range of the op amp and is therefore an important performance parameter. Describe how you will measure the input CMR.

- Closed loop configuration shown on the right. This allows the output to follow the input since the amplifier has a gain of 1 V/V.
- Negative input at V_{mid}
- Positive input at $V_{mid} + V_{cmr}$, where V_{cmr} is the common mode input voltage.
- Perform a DC analysis to vary V_{cmr} from -3 to $+3$ V. This will provide an input at the + terminal that varies from 0 to 6V.
- Plot V_o vs. $(V_{mid} + V_{cmr})$ so that $(V_{mid} + V_{cmr})$ ranges from 0 to 6V.
- The input CMR is the input voltage range $(V_{mid} + V_{cmr})$ for which the output follows the input. Once the output flattens and no longer follows the input, the amplifier is outside of its CMR.

**Problem 4: Output Swing (5pts.)**

The output swing is the range of output voltage for which the output is a linear function of the input ($V_o = A_v V_{in}$). Beyond this range, the output voltage will become non-linear and will saturate at a maximum and minimum output value. This is also known as *clipping* since the output has been “clipped” at a maximum value. Describe how to measure the output swing of an op amp.

- Open loop configuration shown on the right (same as DC gain)
- Negative input at V_{mid}
- Positive input at $V_{mid} + V_{os} + V_{in}$
- Perform a DC analysis to vary V_{in} over a small range around V_{mid}
- Plot V_o vs. V_{in} and note where the output flattens out
- The output swing will be determined by V_{omax} and V_{omin}

**Problem 5: Power Dissipation (5pts.)**

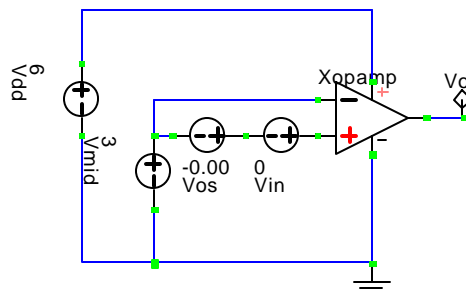
Describe how to measure the power dissipation of the entire circuit, including the bias string(s), using SPICE.

Use any configuration and perform an Operating Point (.OP) analysis. One of the results of this analysis is $I(VDD)$. This is the total current from the power supply which will be the total current used by the circuit. When you multiply $I(VDD)$ by VDD , the result is the total power dissipation of the circuit.

Problem 6: Unity Gain Frequency (10pts.)

At higher frequencies the gain of the op amp will start to fall off due to its limited ability to quickly charge the node capacitances. The unity gain frequency is the frequency of the input signal at which the gain has fallen to a value of 1 V/V or 0 dB. Describe how to measure the unity gain frequency.

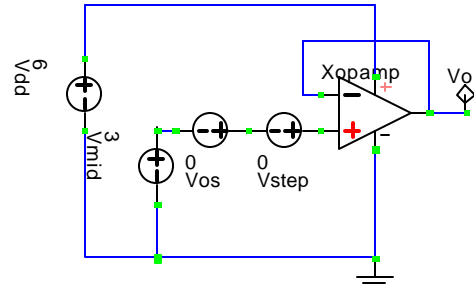
- Open loop configuration shown on the right (same as DC gain)
- Negative input at V_{mid}
- Positive input at $V_{mid} + V_{os} + V_{in}$
- V_{in} is an AC voltage source with DC level of 0V
- Perform an AC analysis to vary frequency of V_{in} from small frequency (~ 10 Hz) to a frequency beyond $A_v = 1$ V/V
- Plot V_o vs. frequency (log scale) and note where $V_o/V_{in} = 1$ V/V or 0 dB.
- The frequency at which this occurs is the unity gain frequency



Problem 7: Settling Time (10pts.)

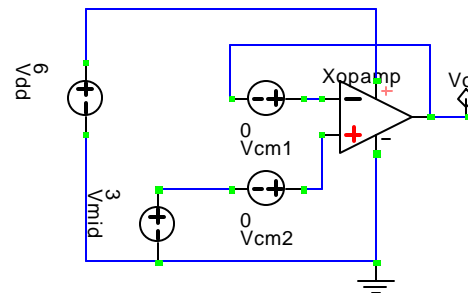
When the DC level at the input of an op amp is changed abruptly, the output voltage will take some time to settle to the new level. This is called the settling time of the circuit. To test this parameter a 1 volt instantaneous step should be applied to the input around V_{mid} (possibly V_{mid} to $V_{mid}+1$) and the time required for V_o to settle to within 0.1% of its stable output level should be measured. Describe how to measure the 0.1% settling time for a 1V input step.

- Closed loop configuration shown on the right so that output will follow input
- Positive input at $V_{mid} + V_{os} + V_{step}$
- V_{step} is a DC pulse starting at 0 V and immediately changing to 1 V
- Perform a Transient analysis
- Plot V_o vs. time and note where V_o is within 0.1% of $V_{mid} + V_{step}$
- The time at which this occurs is the settling time
- Precise values can be found by looking at the output table of values near the point where the output begins to settle to within 0.1% of its final value

**Problem 8: CMRR at DC (10pts.)**

In an op amp, the output should follow the input for any change in common mode signal (same signal at both input terminals) and amplify any differential signal between the two input terminals. The Common Mode Rejection Ratio (CMRR) is a measure of how well the op amp amplifies differential signals relative to amplification of common mode signals. Describe how to measure the CMRR.

- Closed loop configuration shown on the right so that output will follow input
- Positive input at $V_{mid} + V_{cm2}$
- V_{cm1} and V_{cm2} are the common-mode inputs, $V_{cm1} = V_{cm2}$
- V_{cm1} and V_{cm2} are AC sources with DC = 0
- Perform AC analysis over appropriate frequency range
- Plot (V_+ / V_o) in dB, where V_+ is voltage at positive input
- The results show how well the output rejects changes common-mode inputs

**Problem 9: PSRR (10pts.)**

Ideally, the output of an op amp will not change if the power supply voltage varies slightly. The Power Supply Rejection Ratio is a measure of how well the output rejects small changes in power supply voltage. PSRR is a function of frequency so it must be measured over a range of frequencies. Although not specified in the design project description, the performance goal should be stated as >40 dB at 50kHz. Describe how to measure the PSRR of the op amp circuit.

- Closed loop configuration shown on the right so that output will follow input
- Positive input at V_{mid}
- V_{psr} is an AC source applied in series to the power supply
- Perform AC analysis up to 100kHz or so
- Plot V_{ps+} / V_o in dB, where V_{ps+} is the positive power supply node where the V_{psr} connects to VDD of the transistors
- The results show how well the output rejects small changes in the power supply
- Note the PSRR at 50kHz the check performance goal

