

Homework 8

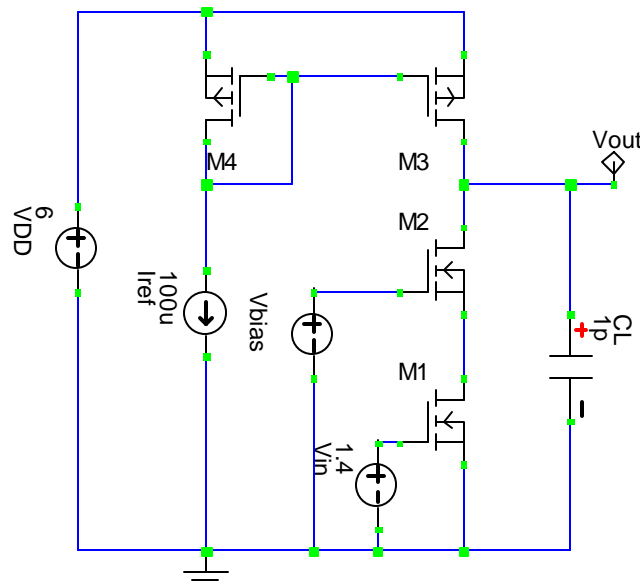
Due: Thursday, 10/26/00

Problem 1: Problem 3.13 from the textbook. You know what the answer is, but you must derive the expression using small signal analysis which includes the body effect by applying the test source method. You may assume that the impedance looking in to the drain of Q2 (Fig. 3.14) is $r_{o2} = r_{ds2}$.

Problem 2: Problem 3.31 from the textbook. The -3dB frequency (in Hertz) is given by $f_{3\text{dB}} = (r_{\text{out}} C_L)^{-1}$.

Problem 3: Cascode Amplifier

The figure below shows an nMOS telescopic cascode amplifier with a pMOS current mirror load, which mirrors a $100\mu\text{A}$ reference current. The transistors have the same parameters used for all previous SPICE problems (repeated below), and the following sizes (W/L in μm): M1: 10/2, M2: 10/2, M3: 5/2, M4: 5/2. VDD is 6V and there is a capacitive load of 1pF.



a) Calculate the required value of V_{bias} if $V_{\text{in}} = 1.4\text{V}$ and $V_{\text{DS1}} = 1.5\text{V}$ (ignore body effect and channel length modulation).

b) Simulate this circuit in SPICE with $V_{\text{in}} = 1.4\text{V}$ and $V_{\text{bias}} = 3\text{V}$. Plot the gain in dB from 10Hz to a frequency slightly greater than the -3dB frequency. List the DC gain and the -3dB frequency. Note, you may need to adjust the maximum frequency to get a good plot, but you can use 10Meg as a starting point.

*As in Homework 7 Problem 4, you will need to use .AC analysis and set source V_{in} to 'Use AC'. To plot the gain in dB, use the expression $\text{DB}(V(x))$ where x is the output node. Note, if you put a marker at the output node and select 'Voltage Probe', this output will probably be automatically selected.

*Set the x-axis to log scale.

*Remove any phase plots from your graph.

- c) Experiment with the effect of the DC level on V_{in} by changing it to 1.3V and 1.5V. Comment on the effects this has on the circuit and why they occur (no SPICE output here, just discuss your observations).
- d) Based on the discussions in class, what feature(s) of this circuit limits the DC gain of this amplifier.

SPICE MOS Model Statements for $L=2\mu\text{m}$ transistors.

```
.model cmosn nmos level = 1 vto = 0.77 kp = 7.7e-5 gamma = 0.71 phi = 0.73  
lambda = 0.0625 tox = 3e-8 ld = 2e-7 u0 = 670 nsub = 2e16  
.model cmosp pmos level = 1 vto = -1.1 kp = 2.1e-5 gamma = 0.355 phi = 0.66  
lambda = 0.053 tox = 3e-8 ld = 5e-8 u0 = 180 nsub = 5e15
```