

## Exam 2

EE 562 Fall 99

*This exam is open book and open notes. You may use any material you bring into the classroom including a calculator. Under no circumstances can you speak to or exchange books, papers, calculators, etc. with other students in the class.*

Total Points: 120

Time: 80 minutes (8am – 9:20am)

- Write your name at the top of the exam and your initials at the top of each sheet.
- Sign the honor pledge at the end of the exam.
- Show all of your work. Try to use only the pages provided (write on back if necessary)
- Give units in your answer.
- Note the point value of each question and try to at least attempt each problem. Partial credit will be given for all calculation problems.

***True or False:*** For each of the following statements, circle T if it is true and F if it is false.  
2 pts. each, 30 points total.

- |   |   |     |   |
|---|---|-----|---|
| T | F | 1.  | A typical CMOS process has less than 10 masking steps.  |
| T | F | 2.  | In SPICE, an Operating Point analysis (.OP) is used to simulate the small signal AC gain of a circuit.  |
| T | F | 3.  | The source/drain to bulk capacitance is due to the existence of a pn-junction within a MOSFET transistor.   |
| T | F | 4.  | The SPICE term PHI represents the potential across the channel (between the substrate and the oxide surface) of an MOS transistor.  |
| T | F | 5.  | If the gate of a transistor is tied (shorted) to the drain, the transistor is always in saturation as long as $V_{GS} > V_t$ .  |
| T | F | 6.  | The common-gate amplifier has an infinite input resistance.   |
| T | F | 7.  | The effect of source degeneration in a common-source amplifier is to increase both $G_m$ and $R_o$ .  |
| T | F | 8.  | A cascode amplifier will have a higher transconductance ( $G_m$ ) than a common-source amplifier with source degeneration.  |
| T | F | 9.  | The gain of an amplifier is often plotted on a decibel, dB, scale.  |
| T | F | 10. | In a source-coupled pair (differential amplifier), the current through each branch is one half of the bias current.   |
| T | F | 11. | Small signal output resistance increases with increasing bias current.  |
| T | F | 12. | In a simple current mirror, decreasing the channel length ( $L$ ) will cause the output current to more closely match the reference current over a broad range of output voltage. |
| T | F | 13. | EE562 is my favorite class.   |



23. Which of the following will increase the gain and decrease the cutoff frequency in an amplifier?

- a) decreasing L
- b) reducing the threshold voltage
- c) increasing the current
- d) increasing W

24. Which of the following is NOT a characteristic of a typical Operational Amplifier? Circle all that apply.

- a) high differential gain
- b) high output resistance
- c) high input resistance
- d) high common-mode gain

25. Which of the following are NOT features of the first stage of an op amp? Circle all that apply.

- a) high gain
- b) common-mode signal rejection
- c) differential-to-single-ended conversion
- d) compensation for stability

**Calculation:** Solve the following problems in the space provided and on the backs of these pages if necessary. You may work on scrap paper, but you must show the major step on these test pages. Unless otherwise stated, use the transistor parameters from the model statements at the end of the exam. (60 points total)

26. SPICE Parameters: Write the appropriate equations for calculating the following Level 1 SPICE parameters for an nMOS transistor. DO NOT CALCULATE THE RESULT. Your equations should be in terms of other SPICE parameters such as NSS, NSUB, TOX, LD, etc., known constants like  $kT$ ,  $n_i$ ,  $\epsilon$ ,  $\epsilon_{OX}$ , etc., and  $\Delta L/\Delta V_{DS}$ .

10 points

a) PHI?

b) VTO?

c) KP?

d) GAMMA?

e) LAMBDA?

27. Common Source Amplifier: This problem deals with a common source amplifier with an nMOS input and a diode-connected pMOS active load. The power supplies are  $V_{DD}=6V$  and ground. The DC voltage is 2 volts at the input and 3 volts at the output. The input transistor has a length of  $L = 2\mu m$ , and you can assume that  $L_{eff} = L$  for both transistors.

20 points

a) Draw the circuit schematic.

b) If the width of the input transistor is  $20\mu m$ , what is the current? Assume, for now, that input nMOS transistor has an infinite output resistance ( $\lambda = 0$ ).

c) What is the W/L ratio of the pMOS load transistor required to keep the output voltage at 3 volts for this current? Assume the current is  $0.5mA$ .

d) What is the transconductance ( $g_m$ ) of this amplifier? Assume the nMOS width is  $20\mu m$  and the current is  $0.5mA$ .

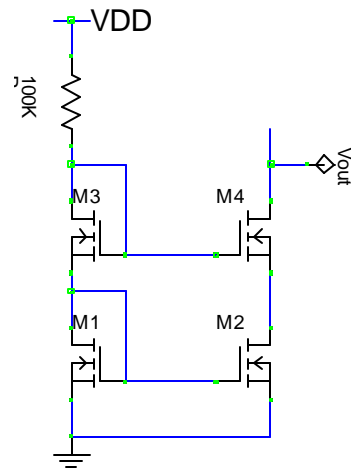
e) What is the output resistance ( $R_0$ ) of this amplifier if  $\lambda_n = 0.02 \text{ V}^{-1}$  and  $\lambda_p = 0.01 \text{ V}^{-1}$ . Assume  $I_D$  is 0.5 mA.

f) What is the voltage gain ( $A_v$ ) of this amplifier?

28. Cascode Current Mirror: The cascode current mirror shown on the right has a resistive load of  $100\text{k}\Omega$ . All four transistors are identical (same  $W/L$ ,  $V_t$ , etc.). Assume  $V_{DD} = 5\text{V}$  and  $L=L_{\text{eff}}$ .

10 points

a) If  $V_{GS} = 1\text{V}$ , what is the bias current?



b) If  $L = 2\mu\text{m}$  for all transistors, what is the width of the transistors? Assume the answer to part (a) was  $50\mu\text{A}$ .

29. Operational Amplifier: A simplified schematic for a two-stage operational amplifier is shown on the right. The input stage is an nMOS differential amplifier with a pMOS active load. The second stage is a pMOS cascode amplifier with an nMOS active load. Assume the following small signal parameters are known:

$$g_{m1} = g_{m2} = 500 \mu\text{A}/\text{V}$$

$$g_{m6} = g_{m7} = 600 \mu\text{A}/\text{V}$$

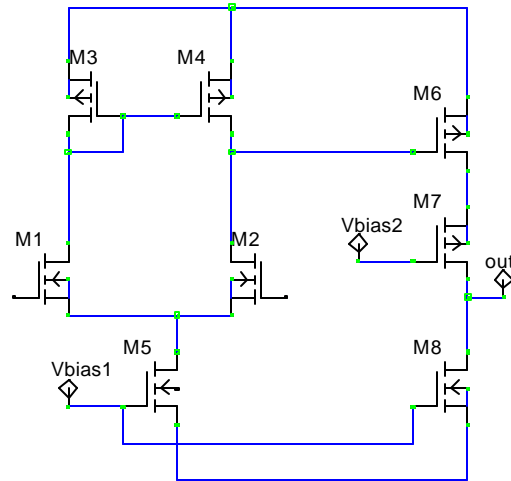
$$r_{o1} = r_{o2} = 500 \text{ k}\Omega$$

$$r_{o3} = r_{o4} = 600 \text{ k}\Omega$$

$$r_{o6} = r_{o7} = 300 \text{ k}\Omega$$

$$r_{o8} = 400 \text{ k}\Omega$$

**20 points**



a) What is the differential gain of the input stage?

b) What is the output resistance of the cascode second stage? Assume the equivalent resistance of M6 and M7 at the output can be approximated by,  $r_{o7} (g_{m7} r_{o6})$ .

c) What is the gain of the second stage?

d) What is the overall gain of the op amp?

***nMOS and pMOS Transistor Model Parameters for calculation problems.***

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.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=2.9200E-08 XJ=0.200000U TPG=1
+ VTO=0.5940 DELTA=5.0730E-01 LD=1.0530E-07 KP=7.9174E-05
+ UO=669.5 THETA=8.2300E-02 RSH=6.5100E+01 GAMMA=0.6546
+ NSUB=1.8050E+16 NFS=7.0240E+11 VMAX=2.1420E+05 ETA=1.3310E-01
+ KAPPA=4.1720E-01 CGDO=1.8679E-10 CGSO=1.8679E-10
+ CGBO=4.3907E-10 CJ=2.8446E-04 MJ=5.2989E-01 CJSW=1.4208E-10
+ MJSW=1.0000E-01 PB=9.8338E-01

.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=2.9200E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8135 DELTA=2.3400E+00 LD=1.1100E-09 KP=2.1464E-05
+ UO=181.5 THETA=1.1800E-01 RSH=1.2080E+01 GAMMA=0.3250
+ NSUB=4.4510E+15 NFS=6.4990E+11 VMAX=2.8250E+05 ETA=1.4560E-01
+ KAPPA=9.9780E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=4.0071E-10 CJ=3.0160E-04 MJ=4.4794E-01 CJSW=1.8785E-10
+ MJSW=1.0476E-01 PB=7.6778E-01
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***Honor Pledge***

*By signing below, I pledge that I have neither given nor received aid on this exam, nor have I witnessed any other student giving or receiving aid.*

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