

NAME: _____

Exam 2

EE 562 Fall 00

During this exam you are allowed to use one sheet of notes and a calculator. You are not allowed to speak to or exchange books, papers, calculators, etc. with other students.

Total Points: 100

Time: 80 minutes (9:30am – 10:50am)

- Write your name at the top of the exam and your initials at the top of each sheet.
- Sign the honor pledge at the end of the exam.
- Show all of your work. Try to use only the pages provided (write on back if necessary)
- Give units in your answers.
- Note the point value of each question and try to at least attempt each problem. Partial credit will be given for all problems involving calculations.

True or False: For each of the following statements, circle T if it is true and F if it is false.

2 pts. each.

T	F	1. The SPICE model parameter LAMBDA is a function of the width (W) of a transistor and should have a different value for each transistor that has a different width.
T	F	2. The .SHOW analysis of SPICE generates several small signal parameters for all transistors in a circuit.
T	F	3. In performing small signal analysis, you must short circuit all DC voltage sources and open all DC current sources.
T	F	4. The input resistance of a common-drain amplifier is approximately $1/g_m$.
T	F	5. The input resistance (looking into the gate) of a diode-connected transistor is infinite.
T	F	6. The output resistance of a transistor with source degeneration is approximately $g_m^2 r_o$.
T	F	7. One advantage of using an nMOS cascode current mirror is that the output voltage can be pulled all the way to ground ($V_{out-min} = 0$).
T	F	8. Increasing the bias current in an amplifier stage will increase the gain and the $-3dB$ frequency.
T	F	9. Of the various parasitic capacitances in a MOSFET, the one that is typically the largest is C_{gs} .
T	F	10. According to the guest lecture, it is important to consider circuit topology (layout view) when doing schematic design.

Multiple Choice: Circle the answer that best fits the question. 3 pts. each.

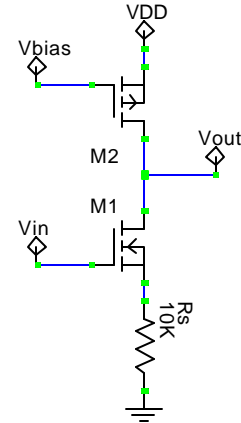
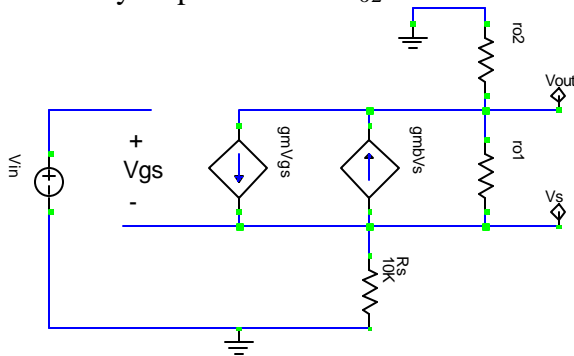
11. Which of the following SPICE analysis methods is best for determining the small signal gain of a circuit?
 a) .OP b) .AC
 c) .DC d) .SHOW
12. Which of the following SPICE analysis methods is best for determining the bias voltages of a circuit?
a) .OP b) .AC
 c) .DC d) .SHOW
13. Which of the following is the amplifier that typically has the highest gain (V_{out}/V_{in})?
 a) common-drain b) Wilson current mirror
c) common-source d) common-gate
14. Which of the following loads would provide the best performance (gain, etc.) for a cascode amplifier?
 a) simple current mirror b) diode connected transistor
 c) resistor d) cascode current mirror
15. Which of the following circuit configurations has the highest output resistance?
 a) common-source amplifier b) common-drain amplifier
 c) Wilson current mirror d) cascode current mirror
16. In the most general form, the gain of a common-source amplifier is not a function of:
 a) transistor gate length b) source/drain area
 c) transistor gate width d) bias current
17. In which of the following can we ignore the small-signal body effect parameter g_{mb} ?
a) common-source amp with $V_{SB}=0$ b) common-drain amplifier with $V_{SB}>0$
 c) common-gate amp with $V_{SB}=0$ d) common-gate amp with $V_{SB}>0$
18. Which of the following will not affect the parasitic junction capacitances in an MOS device?
 a) source/drain area b) gate oxide thickness
 c) substrate impurity concentration d) source/drain voltage
19. In which of the following circuit blocks would you expect the lowest frequency pole?
 a) diode-connected load b) common-source amplifier
c) cascode amplifier d) common-gate amplifier
20. According to the guest lecture, which of the following do not identify “process corners”?
 a) slowest transistors b) supply voltage
 c) fastest transistors d) max. and min. parasitic capacitances

Calculation: Solve the following problems in the space provided and on the backs of these pages if necessary. You may work on scrap paper, but you must show the major steps here. Unless otherwise stated, use the simple SPICE parameters given at the end of the exam.

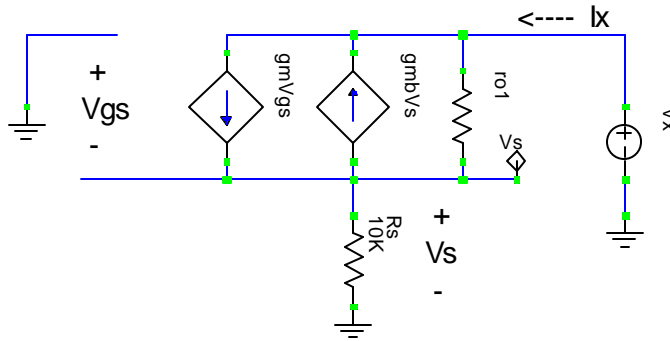
21. Small Signal Modeling:

10 points

a) Draw the complete low frequency small-signal model for the circuit on the right. Assume the pMOS load transistor can be modeled by output resistance r_{o2} .



b) To find an expression for the output resistance looking into the drain of M1 we can ignore transistor M2 and apply a “test source” to the output node. Draw the small signal model for this case. Show the test source and correctly show what you would do to the input (M1 gate).



c) Using KVL and KCL equations, for the circuit in part (b), write expressions for the following in terms of the variables specified:

i) $v_{gs} = f(v_s)$

$$V_{gs} = -V_s$$

ii) $v_s = f(i_x)$

$$V_s = R_s i_x$$

iii) current through r_{o1} , $i_{r_{o1}} = f(v_x, i_x)$ $i_{r_{o1}} = (V_x - V_s) / r_{o1} = (V_x - R_s i_x) / r_{o1}$

which leads to the final step (not required for this problem)

$$i_x = i_{r_{o1}} - V_s(g_m + g_{mb}) = (V_x - R_s i_x) / r_{o1} - R_s i_x (g_m + g_{mb}) \rightarrow V_x / i_x = R_s + r_{o1}(1 + R_s(g_m + g_{mb}))$$

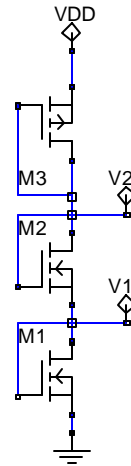
22. DC Biasing: Design a bias voltage generator using a string of diode connected transistors as shown below. Assume for all transistors that $\lambda = 0$ and $V_{SB} = 0$. Note: M3 is pMOS.

10 points

a) If $I_{bias} = 200\mu A$ and $(W/L)_1 = 10/2$ [μm], what is V_1 ?

$$V_1 = V_{GS1} = V_{tn} + \sqrt{\frac{2I_D}{\mu C_{OX}} \frac{L}{W}} = 0.8 + \sqrt{\frac{400\mu}{90\mu} \frac{2}{10}} = 1.74$$

$$V_1 = 1.74V$$



b) Assuming $V_1 = 2V$, what W/L ratio is needed for M2 to generate $V_2 = 4V$ for $I_{bias} = 200\mu A$?

$$V_2 - V_1 = V_{GS2} = 4 - 2 = 2V$$

$$W/L = (2I_D) / (\mu C_{OX} (V_{GS2} - V_t)^2) = (400\mu) / (90\mu (2 - 0.8)^2) = 3.09$$

$$W/L = 3.09$$

c) What V_{DD} is required to meet the conditions of part (b) if W/L of M3 is $22/2$ [μm]?

$$|V_{GS3}| = |V_{tp}| + \sqrt{\frac{2I_D}{\mu C_{OX}} \frac{L}{W}} = 0.9 + \sqrt{\frac{400\mu}{30\mu} \frac{2}{22}} = 2V$$

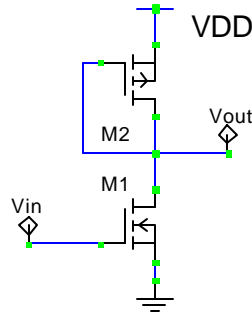
$$V_{DD} = |V_{GS3}| + V_2 = 2 + 4$$

$$V_{DD} = 6V$$

23. Common-Source Amplifier: Analyze an nMOS-input common-source amplifier with a diode connected pMOS load.

10 points

- a) Draw the schematic for this circuit. Label the transistors M1 (input) and M2 (load) and label the input and output.



- b) What is the overall output resistance of this circuit in terms of small signal parameters?
Note: you do not need to perform calculations or small-signal analysis, just define the resistance looking into each device from the output and then express the overall output resistance.

by inspection of the circuit above, $R_{o2} = 1/g_{m2}$, $R_{o1} = r_{o1}$

$$R_{out} = R_{o1} \parallel R_{o2} = 1/g_{m2} \parallel r_{o1} \cong 1/g_{m2}$$

$$R_{out} \cong 1/g_{m2}$$

- c) If the overall output resistance is $50k\Omega$, what is the gain of this amplifier?
Use the following data along with the SPICE parameters at the end of the exam:
 $I_{bias} = 100\mu A$, $(W/L)_1 = 5/2$, $(W/L)_2 = 10/2$.

$$A_v = -g_{m1}R_{out}, \quad R_{out} = 50k\Omega$$

$$g_{m1} = [2 \mu C_{OX} W/L I_D]^{1/2} = [2 \cdot 90u \cdot 5/2 \cdot 100u]^{1/2} = 212\mu A/V$$

$$A_v = -212u \cdot (50k) = -10.6 V/V$$

- d) What is the DC output voltage when the bias current is $200\mu A$ with $V_{DD}=6V$? Assume $(W/L)_2 = 10/2$.

$$|V_{GS2}| = |V_{tp}| + \sqrt{\frac{2I_D}{\mu C_{OX}} \frac{L}{W}} = 0.9 + \sqrt{\frac{400u \cdot 2}{30u \cdot 10}} = 2.53V$$

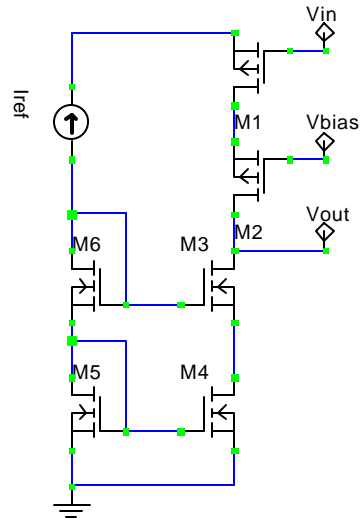
$$V_{out} = V_{DD} - |V_{GS2}| = 6 - 2.53 = 3.47$$

$$V_{out} = 3.47V$$

24. Cascode Current Mirrors and Amps:

10 points

- a) Draw the schematic for a pMOS cascode amplifier with a complete nMOS cascode current mirror load. Assume the source of the current mirror is an ideal current source.
- b) What is the overall output resistance of this circuit if $r_o=200k\Omega$ and $g_m=600\mu A/V$ for all transistors. Briefly explain how you get to your final expression before plugging in numbers.



$$R_{op} \cong r_{op}^2 g_{mp}, R_{on} \cong r_{on}^2 g_{mn}$$

$$R_{out} = R_{op} \parallel R_{on} = r_{op}^2 g_{mp} \parallel r_{on}^2 g_{mn} = \frac{1}{2} r_o^2 g_m$$

$$R_{out} = \frac{1}{2} (200k)^2 (600\mu) = 12M\Omega$$

Rout = 12MΩ

25. Frequency Response: This problem concerns the high frequency response of the circuit shown on the right.

10 points

- a) Express the total capacitance between each of the following node pairs. Be sure to identify which transistor (M1-M3) each capacitance belongs to by using the appropriate subscript.

i) $C_{A-Gnd} = C_L + C_{db1} + C_{gd2} + C_{db2}^*$

ii) $C_{B-Gnd} = C_{gd2} + C_{gd3} + C_{db3} + C_{sb2}^*$

iii) $C_{A-in} = C_{gd1}$

* are valid if M2-bulk is tied to VDD, but not if it is tied to pt. B

- b) Assuming the dominate pole is at Node A, write an expression for the $-3dB$ frequency, ω_{-3dB} , in terms of small signal parameters and parasitic capacitances.

$$R_{out} = R_{o1} \parallel R_{o2} = r_{o1} \parallel r_{o2} g_{m2} / g_{m3} \cong r_{o1} \parallel r_{o2} \cong r_o / 2$$

$$\omega_{-3dB} = (R_{out} \cdot C_{A-Gnd})^{-1}, C_{A-Gnd} \text{ from part a)}$$

$$\omega_{-3dB} \cong 2 / (r_o C_L)$$

- c) If node A is dominated by $C_L=1pF$ and if $r_o=200k\Omega$ and $g_m=600\mu A/V$ for all transistors, what is ω_{-3dB} ?

$$\omega_{-3dB} \cong 2 / (r_o C_L) = 2 / [200k(1p)] = 10Mrad/sec$$

$\omega_{-3dB} \cong 10Mrad/sec$

