

This exam is closed book and closed notes. You may use only this test booklet and your calculator. Any equations or constants you might need are in an equations sheet at the end of the exam. Under no circumstances can you speak to or exchange calculators, etc. with other students in the class.

Total Points: 120

Time: 80 minutes (8am – 9:20am)

- Write your name at the top of the exam and your initials at the top of each sheet.
- Sign the honor pledge at the end of the exam.
- Show all of your work. Try to use only the pages provided (write on back if necessary)
- Give units in your answer.
- Note the point value of each question and try to at least attempt each problem. Partial credit will be given for all problems involving calculations.

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**True or False:** For each of the following statements, circle T if it is true and F if it is false.

2 pts. each.

T	F	1. The photolithography fabrication process involves transferring circuit patterns to a photoresist layer.
T	F	2. Impurity diffusion and thermal oxidation are both done at very high temperatures.
T	F	3. Nonlinear elements in SPICE require a model statement while linear components do not.
T	F	4. The <i>transfer characteristic</i> shows the relationship between the output voltage and the input voltage for an electronics circuit.
T	F	5. Diodes can be used to clip (limit) the maximum swing of the output voltage.
T	F	6. The linear model for a diode with voltage less than $V_f$ is a resistor and a voltage source.
T	F	7. The common-emitter (BJT) and common-source (MOS) inverting amplifiers have a large positive gain.
T	F	8. The effect of replacing the load resistor with a pMOS transistor in an MOS C-S amplifier is to increase the gain but reduce the max and min output voltage.
T	F	9. The small signal gain ( $dV_{out}/dV_{in}$ ) of the BJT and MOS voltage follower are both approximately unity, but the DC magnitude of $V_{out}$ does not equal $V_{in}$ .
T	F	10. The current gain of a common-gate amplifier is approximately unity (1).

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**Multiple Choice:** Circle the answer that best fits the question or statement.

3 pts. each.

11. Which of the following fabrication processes does NOT involve *adding* material to the wafer?

a) metalization

b) doping

c) thermal oxidation

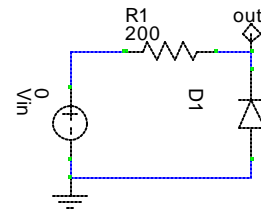
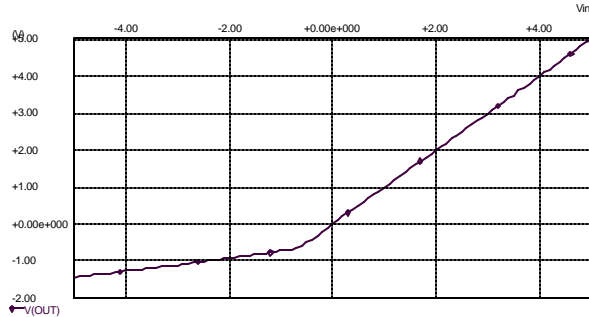
d) reactive ion etching

12. Which of the following materials canNOT be added to a wafer using a *deposition* process?  
 a) metal  b) single crystal silicon  
 c) polysilicon d) dielectrics (oxide, nitride, etc.)
13. Which parameter is NOT part of the SPICE model for a BJT?  
 a) VFBE (turn on voltage of BE junction) b) VAF (forward Early voltage)  
 c) IS (saturation current) d) BF (forward gain factor, beta)
14. Which SPICE parameter models the effect of a source-to-body voltage in a MOSFET?  
 a) LAMBDA  b) GAMMA  
 c) KP d) VTO
15. Which SPICE MOSFET parameter IS *derived* from known base parameters?  
 a) NSUB  b) PHI  
 c) UO d) TOX
16. Which of the following SPICE analysis methods is the best for plotting the transfer characteristic ( $V_{out}$  vs.  $V_{in}$ ) of a circuit?  
 a) DC b) Operating Point  
 c) AC d) Transient
17. Which of the following IS a BJT amplifier configuration?  
 a) common-body b) common-gate  
 c) common-collector d) CMOS inverter
18. A common-drain MOS amplifier has:  
 a) unity current gain b) negative voltage gain  
 c) unity voltage gain d) no gain
19. Consider a common-source nMOS amplifier with an nMOS load. Increasing the width ( $W$ ) of the input transistor will NOT,  
 a) increase the gain b) decrease the minimum output voltage  
 c) increase the size of the circuit  d) decrease the maximum output voltage
20. Which of the following is NOT true for a BJT digital inverter?  
 a) BJT in cutoff for  $V_{in} < V_f$  b)  $V_{OL} = V_{SAT}$   
 c)  $V_{OH} < V_{CC}$  d) gain is negative

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**Calculation:** Solve the following problems in the space provided and on the backs of these pages if necessary. You may work on scrap paper, but you must show the major steps on these test pages.

21. In the diode limiting circuit shown below, resistance R1 is only 200Ω and the diode resistance, rd = 40Ω, cannot be ignored. Draw the transfer characteristic for this circuit from Vin = -5 to 5 V and label the transition voltage(s) as well as the max and min value of Vout (at Vin = 5 and -5V). Assume Vf = 0.7 V. **10 points**  
(draw plot below)



For  $V_{in} < -V_f$ , voltage  $(V_{in} + V_f)$  is divided across  $r_d$  and  $r_d + R_1$

$$V_{out} = -V_f + (V_{in} + V_f) r_d / (R_1 + r_d)$$

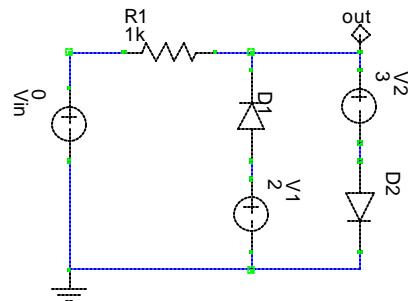
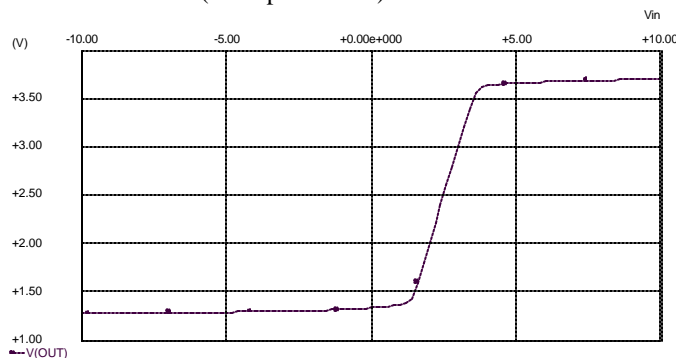
$$\text{for } V_{in} = -5, V_{out} = -0.7 - 4.3(40)/(200 + 40) = -1.42V = V_{out} (-5)$$

For  $V_{in} = -V_f$ , the diode will turn on and  $V_{out} = V_{in}$ , so  $V_{out} (-0.7) = -0.7 V$

For  $V_{in} > -V_f$ , the diode is on and  $V_{out} = V_{in}$ , so  $V_{out} (5) = 5 V$

We can plot these 3 points and connect them with lines to plot the response of this circuit, as shown above.

22. Draw the transfer characteristic of the following diode limiting circuit and label all transition points listed below. Plot from  $V_{in} = -10$  to 10 V. Assume that R1 is much greater than the diode model resistance and  $V_f = 0.7 V$ . **15 points**  
(draw plot below)



Voltage across D1 is  $V_1 - V_{in}$ , so D1 is OFF when  $V_1 - V_{in} < 0.7$ , or  $V_{in} > V_1 - V_f = 1.3V$   
thus D1 is ON for  $V_{in} < 1.3 V$  and OFF for  $V_{in} > 1.3V$ .

voltage across D2 is  $V_{in} - V_2$ , so D2 is OFF when  $V_{in} - V_2 < 0.7$ , or  $V_{in} < V_2 + V_f = 3.7V$   
thus D2 is OFF for  $V_{in} < 3.7V$  and ON for  $V_{in} > 3.7V$

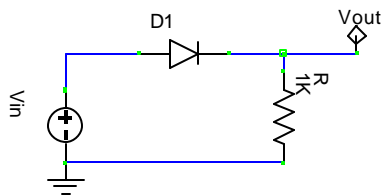
So, for  $V_{in} < 1.3V$ , D1 is on and  $V_{out}$  is held to 1.3V, for  $1.3 < V_{in} < 3.7$  D1 and D2 are off and  $V_{out} = V_{in}$ ,  
for  $V_{in} > 3.7V$ , D2 is on and  $V_{out}$  is held to 3.7V.

What is  $V_{out_{max}}$ ? 3.7 V,  $V_{out_{min}}$ ? 1.3 V, Note,  $V_{out-max/min}$  is same voltage as  $V_{in}$

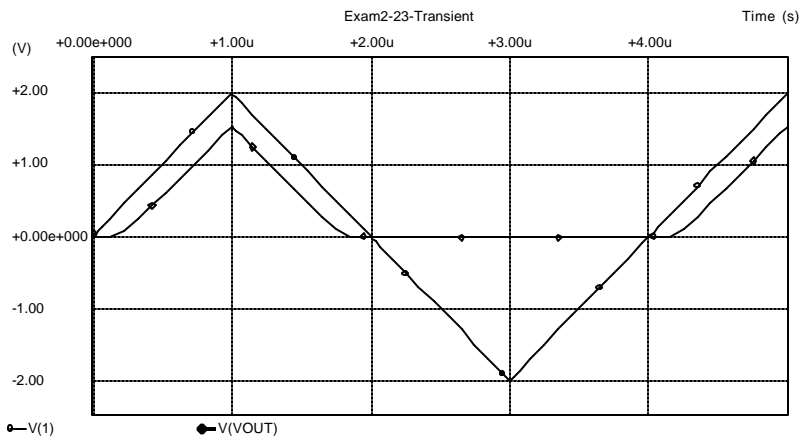
What is the slope ( $V_{out}/V_{in}$ ) between the max. and min. output voltage? 1 V/V ( $V_{out} = V_{in}$ )

23. Half-Wave Rectifier 10 points

Consider the half-wave rectifier circuit shown below. If  $V_{in}$  is a triangle wave with a peak voltage of 2V, and the diode has  $V_f = 0.5V$ , sketch  $V_{out}$  as a function of time on the plot of  $V_{in}$  below. Label the peak voltage of  $V_{out}$ .

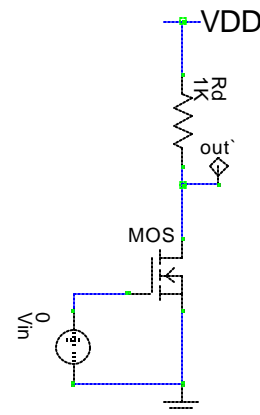


$$\begin{aligned} \text{peak } V_{out} &= V_{in}(\text{peak}) - V_f \\ &= 2 - 0.5 = 1.5 \text{ V.} \end{aligned}$$



24. nMOS Common-Source Amplifier 10 points

(a) Draw an nMOS common-source amplifier with a resistive load,  $R_D$ .



(b) Write the characteristic equations for  $V_{out}$  and  $I_D$  and then express  $V_{out}$  as a function of  $V_{in}$ .

$$\begin{aligned} (1) \quad V_{out} &= V_{DD} - R_D I_D, \\ (2) \quad I_D &= K(V_{GS} - V_{TR})^2, \quad V_{GS} = V_{in} \end{aligned}$$

$$\rightarrow V_{out} = V_{DD} - R_D K (V_{in} - V_{TR})^2$$

(c) If  $R_D = 15k\Omega$  and  $K_n = 3 \text{ mA/V}^2$ , what is the minimum output voltage for which the nMOS transistor remains in saturation? (Hint: you must write the appropriate quadratic equation and find its root). Assume  $V_{DD} = 5 \text{ V}$ .

the transistor will remain in saturation until  $V_{out}$  falls below  $V_{GS} - V_{TR} = V_{in} - V_{TR}$   
So, the question to answer is, when is  $V_{out} = V_{in} - V_{TR}$ ? To do this, substitute  $V_{out}$  for  $V_{in} - V_{TR}$  in the equation above

$$V_{out} = V_{DD} - R_D K (V_{out})^2, \text{ for which we must find the root.}$$

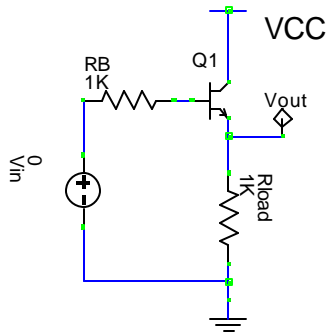
$$\rightarrow \boxed{R_D K V_{out}^2 + V_{out} - V_{DD} = 0} \rightarrow 0 = 45V_{out}^2 + V_{out} - 5$$

$$\text{(the root equation, which could also be written as } \underline{V_{out}^2 + V_{out}/R_D K - V_{DD}/R_D K})$$

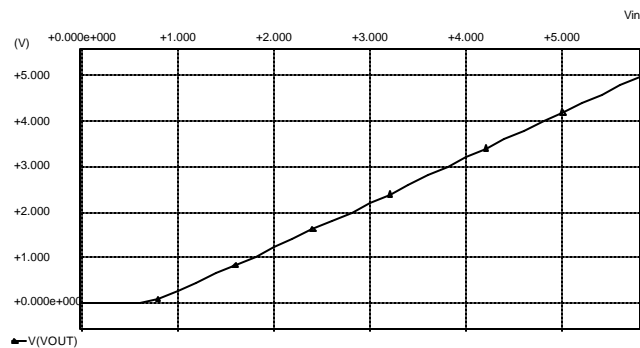
The solution to this equation is  $V_{out} = 0.32 \text{ V}$ .

25. BJT Voltage Follower 10 points

(a) Draw the circuit schematic for a BJT voltage follower with resistive load. Label  $V_{in}$  and  $V_{out}$ .



(b) Sketch the transfer characteristic of this circuit.



Assuming  $V_{f_{BE}} = 0.7 \text{ V}$

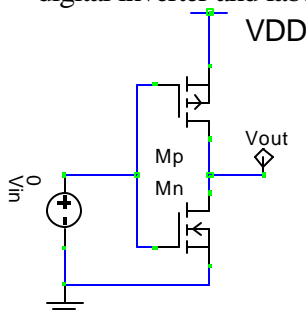
(c) Write an expression for the output voltage that is independent of the load resistance.

$$V_{in} - V(R_B) - V_{f_{BE}} = V_{out}, \quad V(R_B) = i_B R_B$$

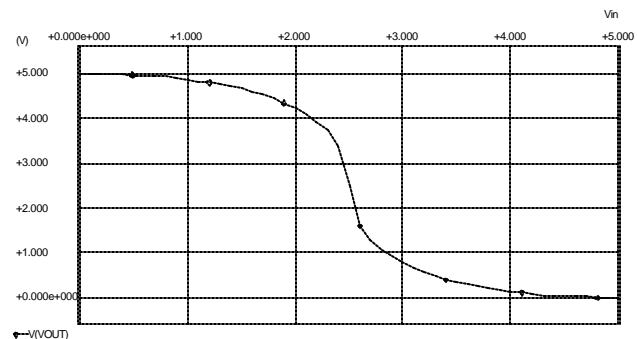
$$\rightarrow V_{out} = V_{in} - V_{f_{BE}} - i_B R_B \quad \text{or} \quad V_{out} = V_{in} - V_{f_{BE}} - i_{load} R_B / (\beta_F + 1)$$

26. CMOS Digital Inverter 15 points

(a) Draw the circuit schematic for a CMOS digital inverter and label  $V_{in}$  and  $V_{out}$ .



(b) Sketch the transfer characteristic of this circuit.



(c) Derive an expression for the input crossover voltage,  $V_{ic}$ . (Hint: Both the nMOS and the pMOS device are in saturation (constant-current) at  $V_{ic}$ .)

At  $V_{in} = V_{ic}$ ,  $I_{Dp} = I_{Dn} \rightarrow K_p (V_{SGp} - V_{TRp})^2 = K_n (V_{GSn} - V_{TRn})^2$ ,  $V_{SGp} = V_{DD} - V_{in}$ ,  $V_{GSn} = V_{in}$   
Solving for  $V_{ic} = V_{in} \rightarrow$

$$\begin{aligned} \rightarrow K_n / K_p &= (V_{DD} - V_{in} - |V_{TRp}|)^2 / (V_{in} - V_{TRn})^2 \quad \text{at } V_{in} = V_{ic} \\ \rightarrow (K_n / K_p)^{1/2} (V_{ic} - V_{TRn}) &= (V_{DD} - V_{ic} - |V_{TRp}|) \\ \rightarrow V_{ic} + (K_n / K_p)^{1/2} V_{ic} &= V_{DD} - |V_{TRp}| + (K_n / K_p)^{1/2} V_{TRn} \\ \rightarrow V_{ic} &= [V_{DD} - |V_{TRp}| + (K_n / K_p)^{1/2} V_{TRn}] / [1 + (K_n / K_p)^{1/2}] \end{aligned}$$

$$\text{or, } V_{ic} = [(K_p / K_n)^{1/2} (V_{DD} - |V_{TRp}|) + V_{TRn}] / [1 + (K_p / K_n)^{1/2}]$$

(d) If  $V_{DD} = 6\text{V}$  and  $V_{ic} = 2\text{V}$ , what is the power consumption of the circuit?

Assume  $V_{TRn} = 1 \text{ V}$  and  $k_n = 0.1 \text{ mA/V}^2$ .

$$I_{Dn} = K_n (V_{GSn} - V_{TRn})^2 = 0.1 (2 - 1)^2 = 100\text{mA} \rightarrow \text{Power} = V_{DD} I_{Dn} = (6)(100\text{m}) = \underline{600 \text{ mW}}$$