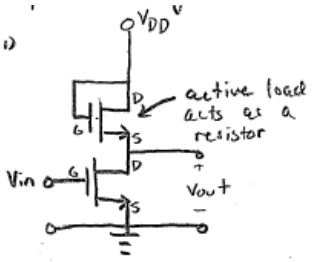
EE462 - Prelab 7 Solution

1.

Truth Tables

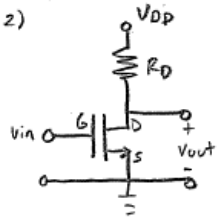
1)



Vin	Vout
0	1
1	0

Logic Inverter

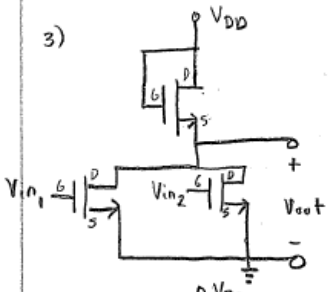
2)



Vin	Vout
0	1
1	0

Logic Inverter

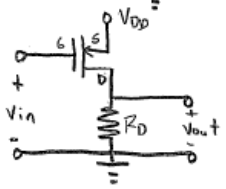
3)



Vin1	Vin2	Vout
0	0	1
0	1	0
1	0	0
1	1	0

Logic Nor

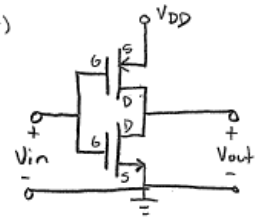
4)



Vin	Vout
0	1
1	0

Logic Inverter

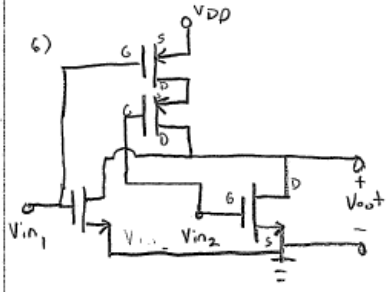
5)



Vin	Vout
0	1
1	0

Logic Inverter

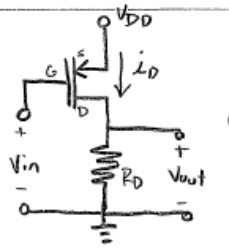
6)



Vin1	Vin2	Vout
0	0	1
0	1	0
1	0	0
1	1	0

Logic Nor

2.



$i_D = 1mA \approx \frac{V_{DD}}{R_D}$ $\therefore R_D = \frac{V_{DD}}{i_D} = \frac{5V}{1mA} = 5k\Omega$

Given: $k_p = .145\ A/V^2$, $V_{TP} = -2.8V$

For logic 1 output, $V_{in} = 0$

$V_{SG} \approx V_{DD} \rightarrow V_{SD} < V_{SG} + V_{TP}$, Triode Region

$$i_D = k_p\left((V_{SG} + V_{TP})V_{SD} - \frac{V_{SD}^2}{2}\right)$$

$$\frac{i_D}{k_p} = (V_{SG} + V_{TP})V_{SD} - \frac{V_{SD}^2}{2}$$

$$\frac{V_{SD}^2}{2} - V_{SD}(V_{SG} + V_{TP}) + \frac{i_D}{k_p} = 0$$

$$V_{SD}^2 - 2(V_{SG} + V_{TP})V_{SD} + \frac{2i_D}{k_p} = 0$$

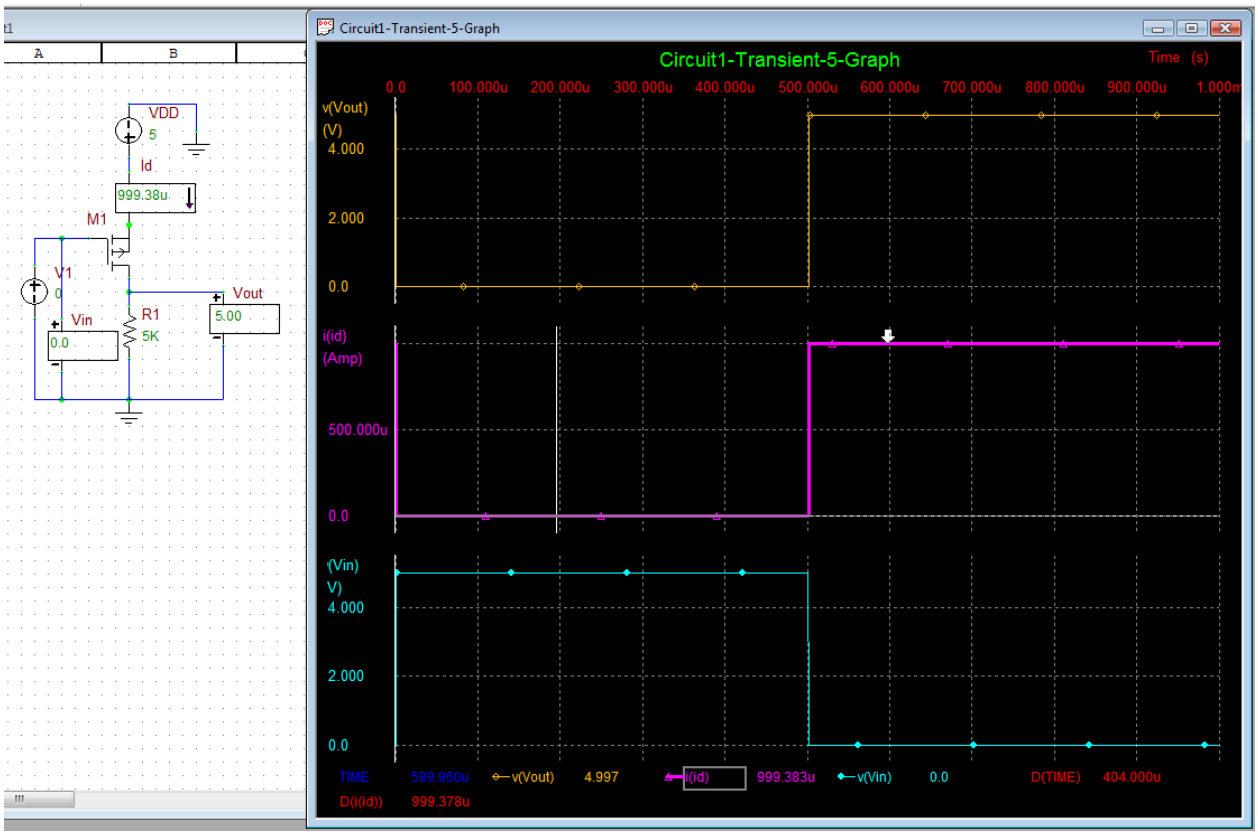
$V_{SD}^2 - 4.4V_{SD} + .013793 = 0$

$\therefore V_{SD} = 4.3969,\ .0031$, $V_{SD} = 3.1mV$

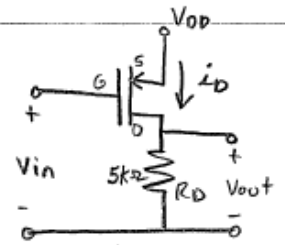
(4.3969 not possible)

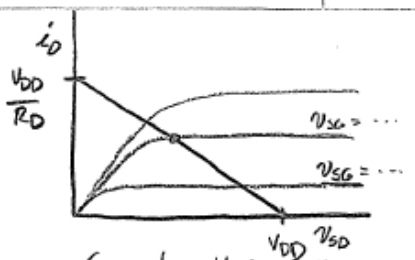
V_{DD}

3)



4)





Load line

$-V_{DD} + V_{SD} + i_D R_D = 0$

$i_D = \frac{V_{DD} - V_{SD}}{R_D}$

$\therefore i_D = 0, \quad V_{DD} = V_{SD}$

$V_{SD} = 0, \quad i_D = \frac{V_{DD}}{R_D}$

Generate Vout vs Vin:

Find where load line intersects MOSFET curves to find i_D and thus Vout, where $V_{out} = i_D R_D$

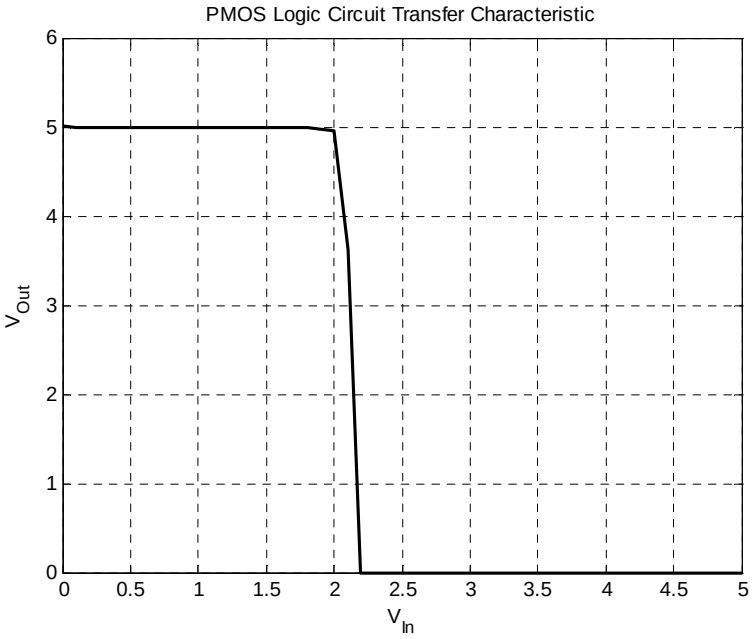
MOSFET

$V_{SG} = V_{DD} - V_{in}$

$V_{in} = 0$ to $5V$

$K_p = .145$

$V_{TP} = -2.8$




```
% EE462 - Prelab 7 - Problem 4
% Stephen Maloney

clear all; close all; clc;

% Set up P-MOS Mosfet Parameters
KP = .145;
VTP = -2.8;

% Set up circuit values
RD = 5E3;
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```
VDD = 5;

% A very fine VSD is required for accuracy
VSD = 0:1E-5:5;

% Load line generated by resistor RD
ILL = -1/RD*VSD + VDD/RD;

% Sweep input voltage from logic low (0) to logic high (5)
VIN = 0:.1:5;

% Run through all input voltages and find the Q points where the load
% line and MOSFET curve intersect. The smallest error point is the Q point,
% representing the particular current at that input voltage.

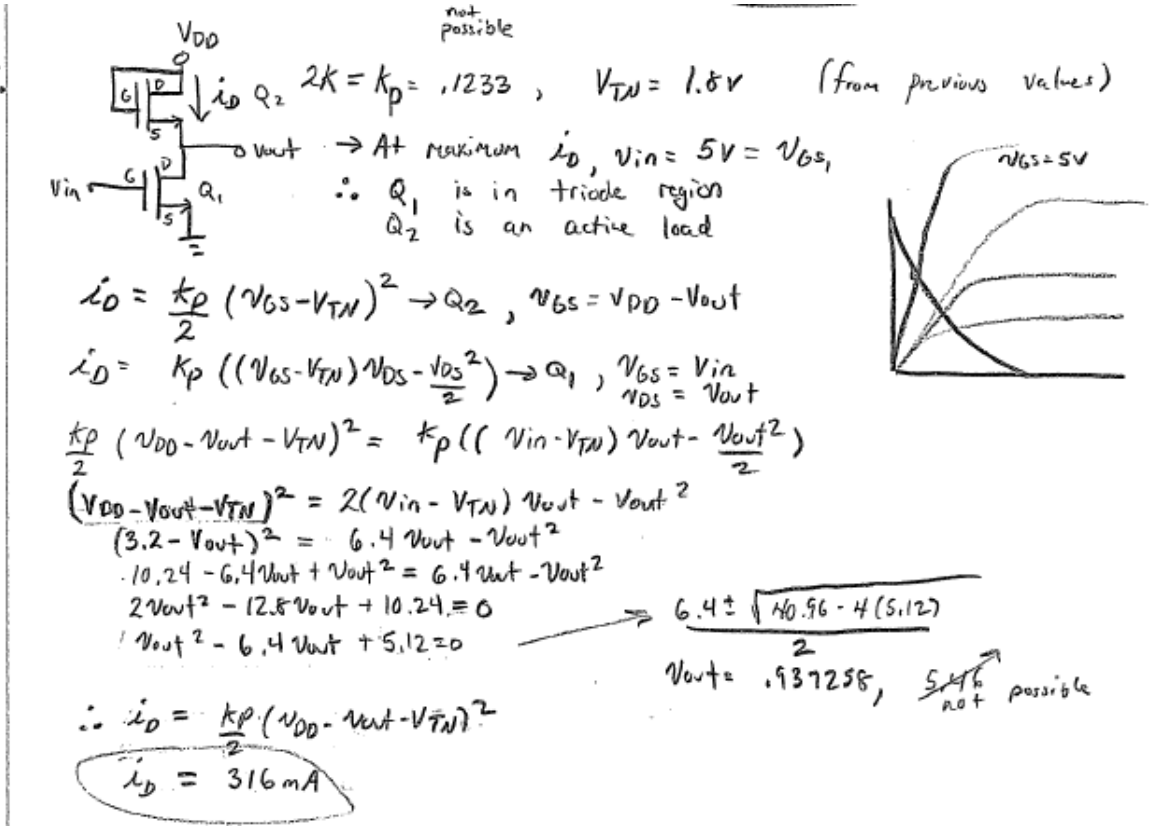
for K = 1 : length(VIN)
    VSG = VDD - VIN(K);

    % Use the NMOS routine to generate ID curve.
    % Note that the VSD and VSG must be used for the PMOS mosfet
    ID = nmos(VSD, VSG, KP, 1, 1, -1*VTP);
    [Error, Eindex] = min(abs(ID - ILL));
    IDMatch(K) = ID(Eindex(1));

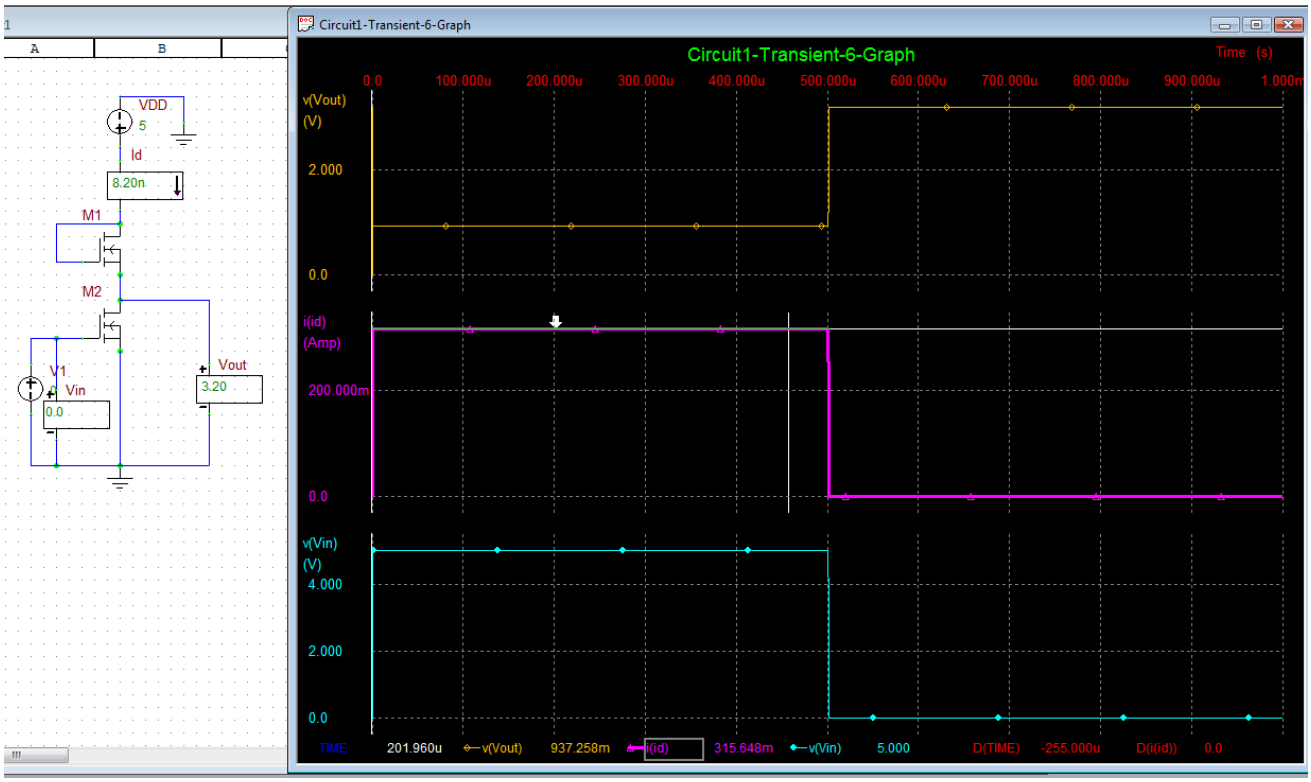
end

% Calculate the output voltage
VOUT = IDMatch * RD;

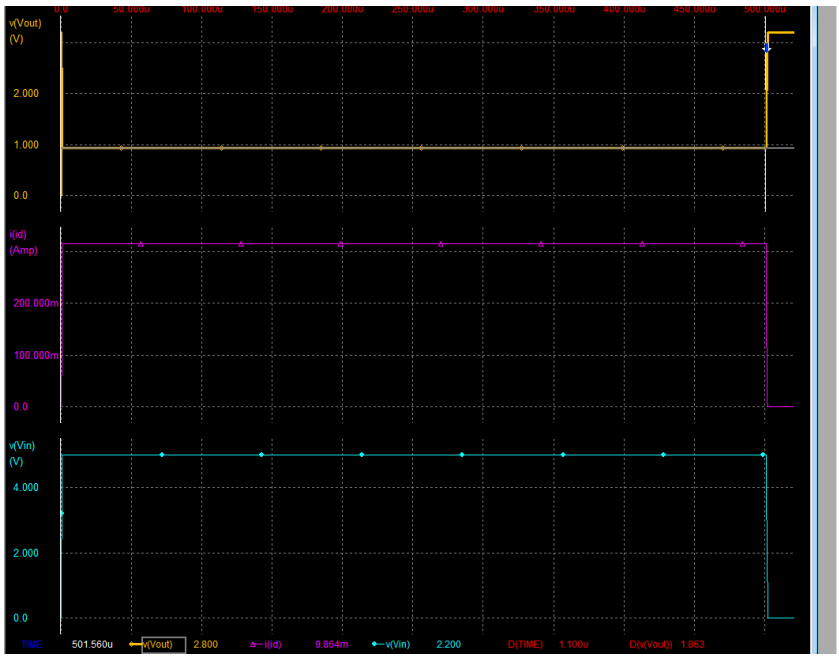
% Plot transfer characteristic
plot(VIN, VOUT, 'k', 'LineWidth', 2); grid on;
title('PMOS Logic Circuit Transfer Characteristic'); xlabel('V_{In}');
ylabel('V_{Out}');
```



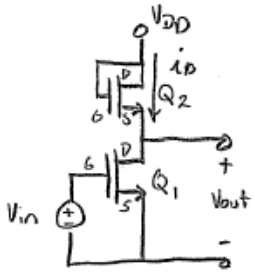
6)



Peak power can approximately found by moving the cursor on the graph into the switching event. As seen below, about 27mW is the peak power for this value of K_p and V_{tn}.

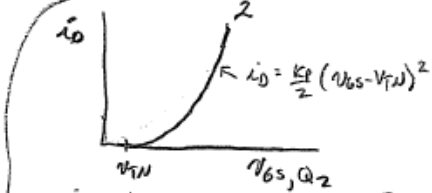


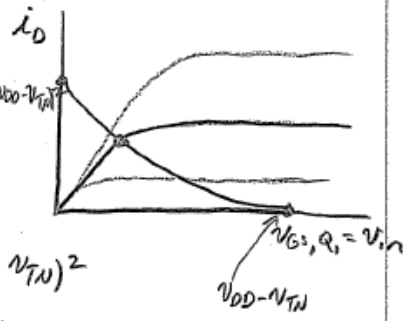
7)



Q_2 is an active load, thus $v_{DS} > v_{GS} - V_{TN}$ always.

$\therefore i_D = \frac{K_P}{2}(v_{GS} - V_{TN})^2$, where $v_{GS} = v_{DS} = v_{DD} - v_{out}$





$i_D = \frac{K_P}{2}(v_{DD} - v_{out} - V_{TN})^2$

$v_{out} = v_{DSQ_1} \rightarrow i_D = \frac{K_P}{2}(v_{DD} - v_{DSQ_1} - V_{TN})^2$

$\therefore v_{DSQ_1} = 0,\ i_D = \frac{K_P}{2}(v_{DD} - V_{TN})^2$

$i_D = 0,\ v_{DSQ_1} = v_{DD} - V_{TN}$

Load line

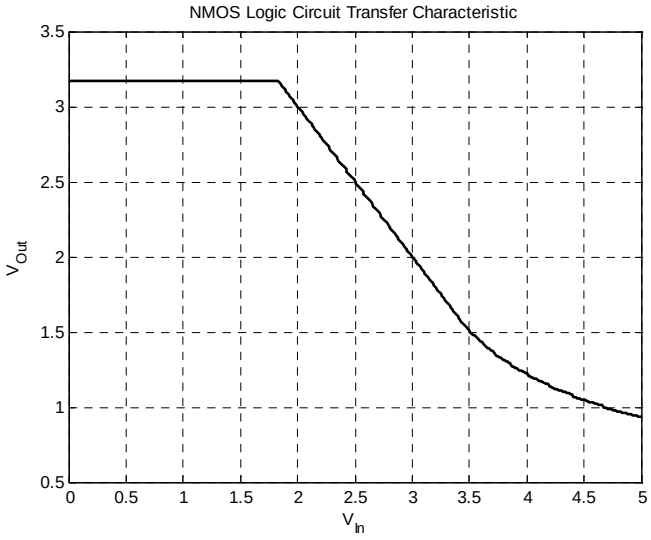
$i_D = \frac{K_P}{2}(v_{DD} - V_{TN} - v_{DSQ_1})^2$

MOSFET

$v_{GS} = v_{in}$

$K_P = .1233$

$V_{TN} = 1.8$




```
% EE462 - Prelab 7 - Problem 7
% Stephen Maloney

clear all; close all; clc;

% Set up N-MOS Mosfet Parameters
KP = .101;
VTN = 1.833;

% Set up circuit values
VDD = 5;

% Sweep input voltage from logic low (0) to logic high (5)
VIN  = 0:.01:5;
```

```
VDS  = 0:.01:5;

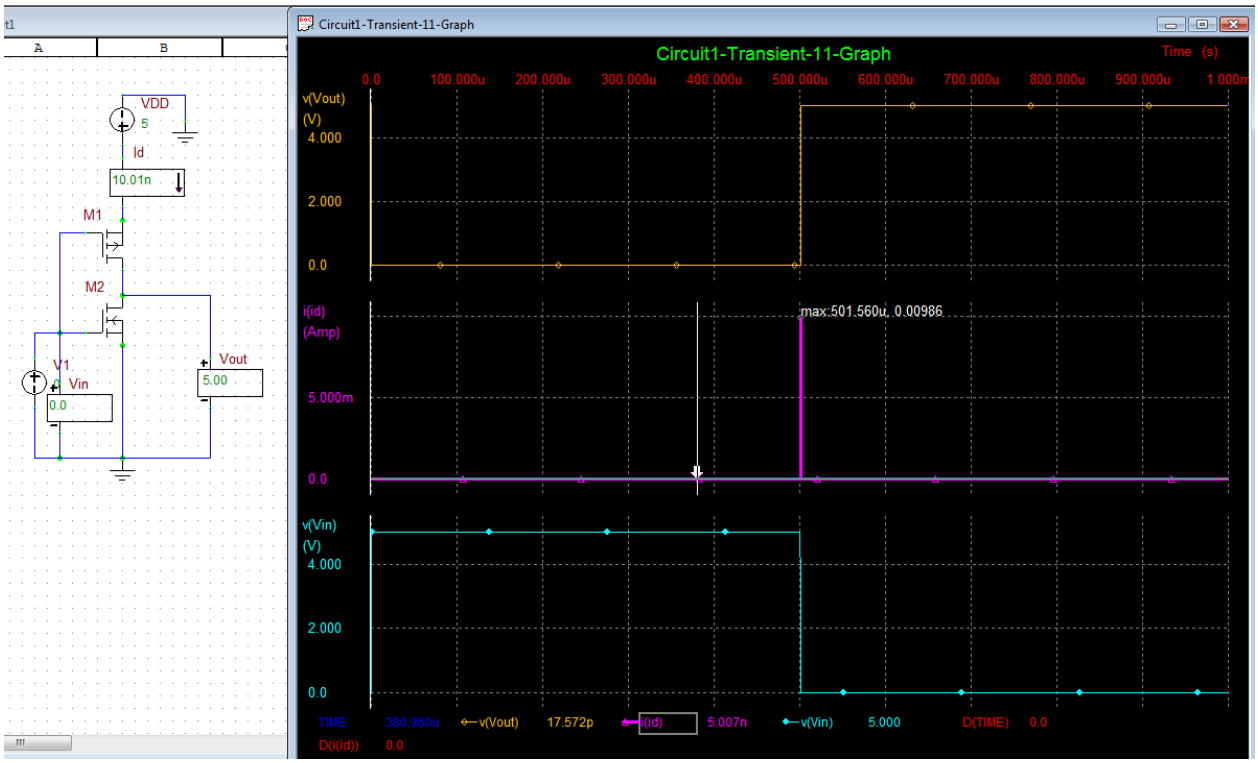
% Set up square law device load line
% It is zero on the far side of VDD-VTN
VOUTSP = 0:.01:VDD-VTN;
IDQ1GEN = KP/2*(VDD - VOUTSP - VTN).^2;
IDQ1 = [IDQ1GEN, zeros(1, length(VDS) - length(IDQ1GEN))];

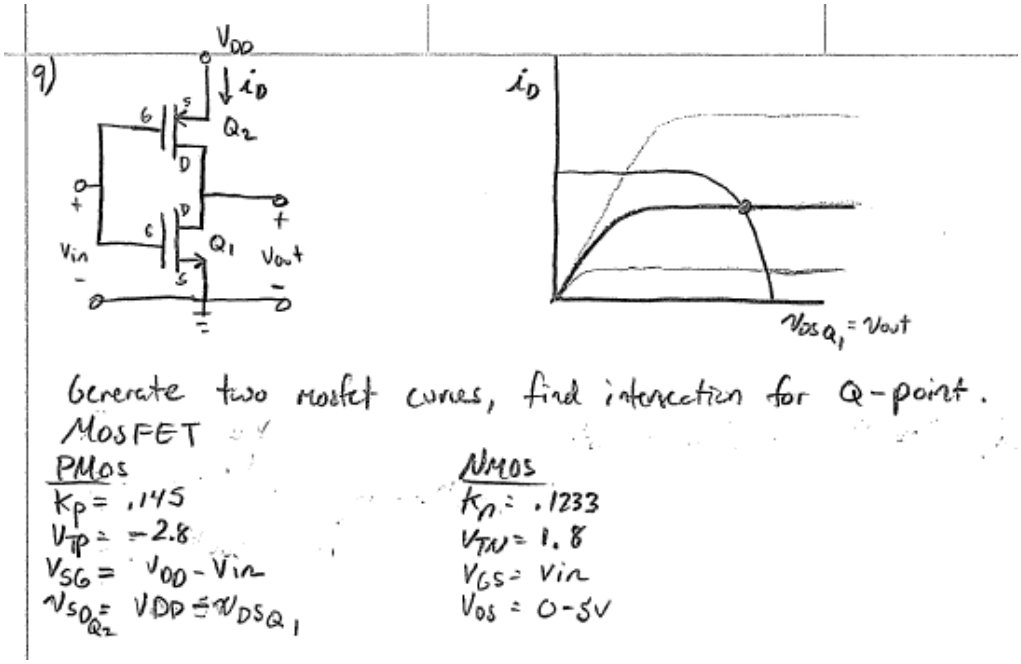
disp('Generating TC...');

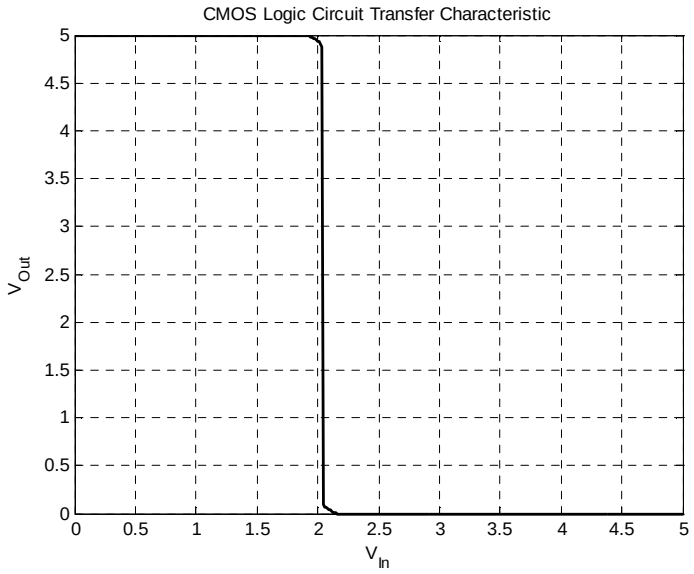
% Run through the input voltage values (VGS of the second mosfet)
% And see where the load line and the MOSFET curve intersect
for K = 1 : length(VIN)
    IDQ2 = nmos(VDS, VIN(K), KP, 1, 1, VTN);
    [Error, Eindex] = min(abs(IDQ1 - IDQ2));
    IDMatch(K) = IDQ2(Eindex(1));
    VDSMatch(K) = VDS(Eindex(1));
end

% Display final transfer characteristic
plot(VIN, VDSMatch, 'k', 'LineWidth', 2); grid on;
title('NMOS Logic Circuit Transfer Characteristic');
xlabel('V_{In}'); ylabel('V_{Out}');
```

8)








```
% EE462 - Prelab 7 - Problem 9
% Stephen Maloney

clear all; close all; clc;

% Set up N-MOS Mosfet Parameters
KP_N = .101;
VTN = 1.833;

% Set up P-MOS Mosfet Parameters
KP_P = .145;
VTP = -2.8;

% Set up circuit values
VDD = 5;
```

```
disp('Generating TC...');

% Sweep input voltage
VIN = 0:.01:5;
VDS = 0:.01:5;
VSD = VDD-VDS;

for K = 1 : length(VIN)
    % The PMOS can be treated as an NMOS by creative subscript use
    IDQ2 = nmos(VSD, VDD-VIN(K), KP_P, 1, 1, -1*VTP);
    IDQ1 = nmos(VDS, VIN(K), KP_N, 1, 1, VTN);

    % Find where the two curves intersect for the q-points
    [Error, Eindex] = min(abs(IDQ1 - IDQ2));
    IDMatch(K) = IDQ1(Eindex(1));
    VDSMatch(K) = VDS(Eindex(1));

    % DEBUG - Uncomment below to view intersection plot
    %plot(VDS, IDQ2, VDS, IDQ1, VDSMatch(K), IDMatch(K), 'o', 'LineWidth', 2);
    %title(['VIN = ' num2str(VIN(K))]);
    %pause(.0001);
    % END DEBUG
end

% Display final transfer characteristic
plot(VIN, VDSMatch, 'k', 'LineWidth', 2); grid on;
title('CMOS Logic Circuit Transfer Characteristic');
xlabel('V_{In}'); ylabel('V_{Out}');
```