EE462G: Laboratory Assignment 7
NMOS and CMOS Logic Circuits

by
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I. Instructional Objectives

- Build and measure parameters of an NMOS logic circuit
- Build and measure parameters of a CMOS logic circuit
- Understand the advantages of CMOS logic circuits

See 6.4.4, 6.4.5, and 14.2 in Horenstein

II. Background

A simple logic inverter can be built using an N-channel MOSFET and a drain resistor as shown in Fig. 1. An alternative configuration using a P-channel MOSFET and a drain resistor is shown in Fig. 2. These inverter configurations serve as a useful introduction to transistors as digital devices, but they are no longer used in practical logic circuits. Active MOS transistors are used in place of the resistors due to their smaller size and lower power dissipation. Thus, modern logic circuits are made up entirely of transistors. Transistor-only logic circuits can be designed using only N-channel MOSFETs, in which case the circuits are called NMOS circuits. Alternatively they can be designed using both N-channel and P-channel MOSFETs, in which case they are called complimentary MOS or CMOS circuits. While the NMOS circuits are faster than the CMOS circuits, the CMOS circuits use less power and as a result have become more common.

NMOS

The key to NMOS circuit designs is the diode-connected NMOS transistor. In the case of the NMOS logic inverter in Fig. 3, the transistor plays the same role as the pull-up resistor (R_D) in the inverter circuit of Fig. 1. By connecting the MOSFET's gate to its drain ($V_{GS} = V_{DS}$), as done in Figs. 3 and 4, the MOSFET transistor operates in its saturation region since $V_{DS} \geq V_{GS} - V_{tr}$ unless it goes into cutoff. Connected in this way, the N channel MOSFET supplies a constant current to the other transistors in the logic circuit, which serve as voltage controlled switches that direct the flow of current. If a digital *high* is present on the gate, current flows through the device. When a digital *low* is present on the gate, current cannot flow through the device and must flow elsewhere. If current is "sinked" to ground through a transistor, the output of the logic circuit is low. If current does not reach ground, it must flow out of the logic circuit, thus providing a logic high output. Another MOS logic circuit example is shown in Fig. 4.

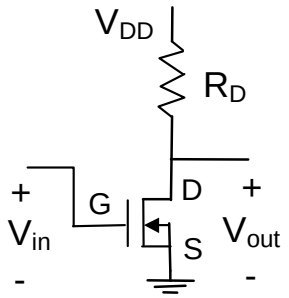

Figure 1. NMOS Logic Inverter Circuit with a pull-up resister.

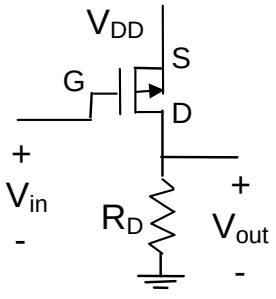

Figure 2. PMOS Logic Circuit with a pull-down resister.

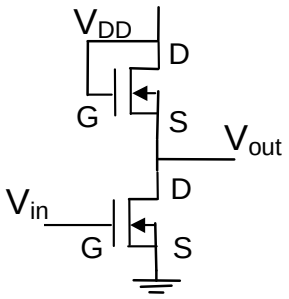

Figure 3. NMOS Logic Inverter Circuit.

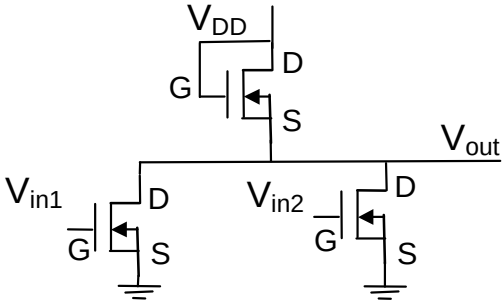

Figure 4. NMOS Logic Gate Circuit.

CMOS

Complementary MOS circuits use both N-channel and P-channel MOSFETs. In the case of the CMOS logic inverter in Fig. 5, the P-channel MOSFET plays the same role as the pull up resistor (R_D) in the inverter circuit in Fig. 1. Note that when the input is low (0V) the N-channel MOSFET is off and the P-channel MOSFET is on (note its V_{GS} = $-V_{DD}$) . Thus, the output is high. When the input is high (V_{in}=V_{DD}) the P-channel MOSFET is off (its V_{GS} = 0V) and the N-channel MOSFET is on. Thus, the output is low.

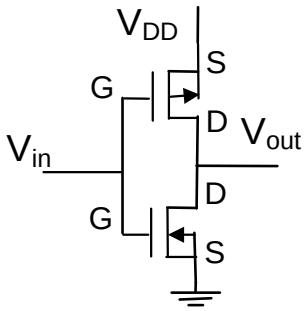

Figure 5. CMOS Logic Inverter Circuit

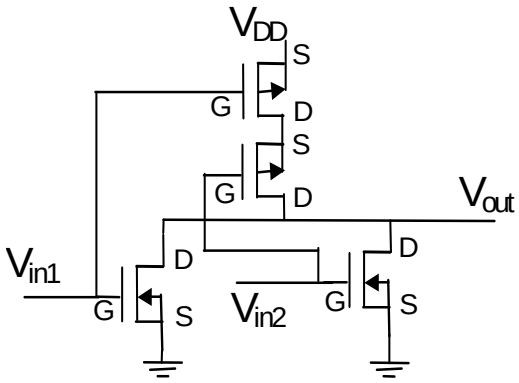

Figure 6. CMOS Logic Gate Circuit

III. Pre-Laboratory Exercises

For the N-channel MOSFET ZVN3306A use the values for K_p and V_{tr} that you used in previous labs. For the P-channel MOSFET ZVP3306A, let $K_p = 2K = 0.145$ A / V^2, and $V_{tr} = -2.8$ V. For the N-channel MOSFET you can use values you estimated in the previous labs. Let $V_{DD} = 5$ V. Let the input voltage be 0V for a logic zero and 5V for logic 1.

Truth Tables for Logic Circuits:

1. Determine the truth tables for each circuit in Figs. 1 through 6 and indicate the logic function of each circuit.

Circuit Transfer Characteristics for PMOS logic:

2. For the circuit in Fig. 2 choose R_D so that the drain current is approximately 1mA with a logic 1 output voltage and determine the value of V_{SD} under this condition.
3. Use SPICE to simulate the circuit in Fig. 2 with the R_D value calculated in the previous problem (use the MOSFET-> empty level 1 PMOS model, set the necessary parameters, and flip it vertically). Use a 1kHz, 0V to 5V square wave (called pulse on B2SPICE options; a square wave has a 50% duty cycle, meaning on half the time, off half the time) with 1μs rise and fall times. Plot the input voltage and the output voltage. Also plot the current from the V_{DD} source.

4. Write a Matlab program to compute and plot the transfer characteristics for the circuit of Fig. 2 with the R_D value used in the previous problem. Hand in the plot and a printout of the commented program used to generate it. (Hint: find the q point as you sweep the input voltage by comparing the load line equation to the MOSFET curve at that particular V_{SG} value (mean squared error), store the found I_D value for each of the input voltage points, and use it to find V_{out}. Finally, plot V_{out} Vs. V_{in}.)

Circuit Transfer Characteristics for NMOS logic:

5. For the circuit in Fig. 3, determine the maximum drain current.
6. Use SPICE to simulate the circuit in Fig. 3. Use a 1kHz, 0V to 5V pulse with 1μs rise and fall times. Plot the input voltage and the output voltage. Also plot the current from the V_{DD} source. Determine the peak (instantaneous) output power during the input pulse transitions (switching events).
7. Write a Matlab program to compute and plot the transfer characteristics for the circuit of Fig. 3. Hand in the plot and a printout of the commented program used to generate it.

Circuit Transfer Characteristics for CMOS Logic:

8. Use SPICE to simulate the circuit in Fig. 5. In this case, use K_p = .1233 for both PMOS and NMOS MOSFETs; also use V_{tp} = -1.8 and V_{tn} = 1.8 (in CMOS configuration, typically the MOSFETS are engineered to match for power consumption purposes). Use a 1kHz, 0V to 5V pulse as input with 1μs rise and fall times. Plot the input voltage and the output voltage. Also plot the current from the V_{DD} source. Zoom in on the current plot around a switching event and determine the peak current during a switching event (or use show next maximum on the edit menu).
9. Write a Matlab program to compute and plot the transfer characteristics for the circuit of Fig. 5. Hand in the plot and a printout of the commented program used to generate it.

IV. Laboratory Exercise

1. **Obtain transfer characteristic of circuit in Fig. 2:** Use the oscilloscope with appropriate setting to obtain the circuit's TC. Determine the value of the threshold voltage for V_{GS} from the circuit's TC. Record the circuit's transfer characteristic and indicate the point on your plot that you used to determine the threshold value of V_{GS}. (**Discussion: Compare to specified values used in prelab. Based on the TC curve determine good values for V_{OH}, V_{OL} , V_{IH}, and V_{IL}. Explain your reasoning.**)
2. **Measure Supply current for circuit in Fig. 2:** Apply a 0 to 5 volt square wave at 1 kHz and record a voltage proportional to the V_{DD} supply current. Determine the current's maximum and minimum values? (**Discussion: When does the inverter draw the most power?**)
3. **Obtain transfer characteristic of circuit in Fig. 3:** Use the oscilloscope with appropriate setting to obtain the transfer characteristic. Determine the value of the threshold voltage for V_{GS} from the circuit's transfer characteristic. Record the circuit's transfer characteristic and indicate the point on your plot that you used to determine the threshold value of V_{GS}. (**Discussion: Compare to specified values used in prelab. Based on the TC curve determine good values for V_{OH}, V_{OL} , V_{IH}, and V_{IL}. Explain your reasoning.**)
4. **Measure Supply current for circuit in Fig. 3:** Apply a 0 to 5 volt square wave at 1 kHz and record a voltage proportional to the V_{DD} supply current. Determine the current's maximum and minimum values. (**Discussion: When does the inverter draw the most power?**)
5. **Observe junction capacitance effects:** For the circuit in Fig. 3, record the output voltage for input square waves at 1kHz and 10kHz input voltages. (**Discussion: Explain the results. Provide reasons for differences at the two frequencies.)**
6. **Obtain transfer characteristic of circuit in Fig. 5.** Measure and record the circuit's transfer characteristic and indicate on your plot where V_{GS} of the n-channel MOSFET is equal to its threshold voltage and where V_{GS} of the p-channel MOSFET is equal to its threshold voltage. From the transfer characteristics determine good values for the inverter's V_{OH}, V_{OL}, V_{IH}, and V_{IL}. (**Discussion: Explain why results differ from previous inverter circuits.**)
7. **Observe effect of decoupling capacitor:** Input a 100kHz square wave, 0V to 5V, into the CMOS inverter circuit in Fig. 5. Record V_{out} and V_{in} to demonstrate your circuit inverts the input. Especially note V_{out} at the edges of the transitions from high to low and low to high. Expand your scope trace around these transitions. Next, place a capacitor (on the order of 0.1μF) from the 5V V_{DD} to ground close on your circuit board. A

capacitor used this way is called a decoupling capacitor. Note that the capacitors used in your amplifiers were called coupling capacitors not decoupling capacitors. They are different and serve a different function. In an ideal circuit with an ideal DC source, decoupling capacitors would have no effect. (**Discussion: Explain why V_{out} changes in this circuit as a result of the capacitor.**) Repeat with a capacitor on the order of 10μF. (**Discussion: Describe the differences between the effects of the smaller and the larger capacitors.**)

8. **Observed drain current properties:** For the CMOS circuit in Fig. 5, put a 10Ω resistor from the source of the lower NMOS transistor and ground to measure the V_{DD} supply current. Input a 1 MHz square wave, 0V to 5V. Record the supply current waveform for one cycle (1μs). Next expand your waveform around a single switching event where the output goes high and record the waveform. What is the peak current? Next expand your waveform around a single switching event where the output goes low. What is the peak current now? (**Discussion: What advantage is apparent for CMOS logic circuits?**)
9. **Measure propagation delay:** Measure the rise time, the fall time and the delay time (average between turn on and turn off delays) as defined in Fig. 7 for the CMOS inverter with the decoupling capacitor in your circuit (any value). You will have to trigger on the positive edge and then the negative edge of the input voltage and display both V_{out} and V_{in} simultaneously. Expand the waveforms using the horizontal time per division adjust. (**Discussion: What would be the highest frequency to clock your circuit at? Explain.**)

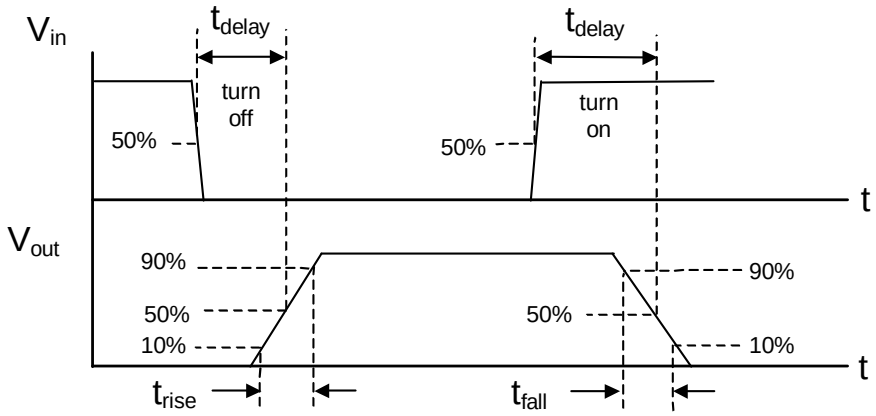

Fig. 7. Definitions of delay, rise, and fall time