Questions for Lab Report:

- **What is the purpose of decoupling capacitors (in parallel with the DC power supply) in CMOS logic circuits?**

- **In theory, if the C-MOS inverter were supplied with a true square wave input then a decoupling capacitor would have no effect.**
- **However, most square waves are composed of a large number of superimposed sine waves with different frequencies. The resulting signal is an approximation of a square wave that varies most dramatically from a true square wave near the transitions.**
- **When a square wave approximation is supplied to the input the transition harmonics cause harmonics in the output. A decoupling capacitor resists these changes and damped the harmonics.**

Questions for Lab Report:

- **What factors determine the highest clock speed at which a logic gate can reliably be driven?**

  $T=t_{PD}=(tf_{delay}+tr_{delay})/2$

  Clock speed: f=1/T