EE 462: Laboratory Assignment 5
Biasing N- channel MOSFET Transistor

by
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I. Instructional Objectives

- Analyze the metal oxide semiconductor (MOS) field effect transistor (FET) (MOSFET) using a DC load line
- Design a circuit to set a DC operating point for a MOSFET
- Measure the operating points in a DC biased FET circuit
- Become more familiar with programming in LabVIEW

(See Horenstein 5.2, 7.3.1, and 7.3.3)

II. Background

Transistors are nonlinear devices; however, over certain operating regions they can be approximated with linear models. To ensure a transistor operates in its linear region, a DC level is added to its input signal. The design of this DC level is referred to as biasing the transistor. The DC current and voltage values are referred to as the transistor's DC operating point (or its bias point) (or its quiescent point). Once a transistor is biased in a linear region, small changes for the input currents and voltages around the bias point will cause the outputs to change in a linearly proportional manner (approximately). It is assumed that the variation of the transistor's currents and voltages are small enough such that they do not move the system into nonlinear operation regions (triode region or cutoff).

The simplest common source MOSFET amplifier biasing scheme is shown in Fig. 1. Since only the DC operating point is of interest right now, the time varying part of the input signal is omitted. The actual signal would be an AC signal added to the V_{GG} (Gate to Ground DC signal). The transfer characteristic (output as a function of the input) for this circuit can be derived. Apply KVL in Fig. 1 to obtain:

$$V_{out} = V_{DD} - R_D I_D \,, \qquad (1)$$

then using a relationship between I_D and the gate voltage V_{GG} when the MOSFET is in the saturated (forward active) region, Eq. (1) becomes:

$$V_{out} = V_{DD} - R_D \frac{K_p}{2}\left(V_{GG} - V_{tr}\right)^2 \text{ where } \frac{K_p}{2} = K \qquad (2)$$

(Horrenstein uses K and Spice uses K_p).

and V_{tr} is the threshold voltage between the cutoff and triode operation region.

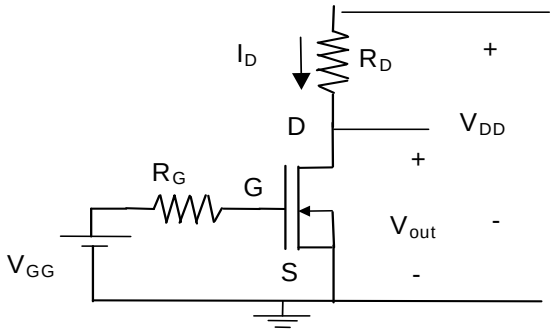

Fig. 1 Basic common source amplifier biasing.

The operating points of V_{GG} and V_{out} are the DC or quiescent values at the input and output, respectively. Ideally, for a certain value of V_{GG}, V_{out} should always result in a corresponding value that does not change. However this relationship will change due to temperature variations or manufacturing variability. Unfortunately the MOSFET's transconductance parameter K_p cannot be controlled well during manufacturing. In addition, K_p also varies with temperature. Some transistor's K_p can vary by more than a factor of 3. Note that K_p is not directly specified in the data sheet but rather the transconductance g_m is specified. The relationship between the MOSFET's transconductance g_m and K_p will be addressed in future labs. Since K_p varies significantly, a circuit biased correctly for one transistor may not be biased correctly for another transistor, even for one with the same manufacture and part number. Therefore, a more robust biasing scheme than the one shown in Fig. 1 is needed, such that the MOSFET's quiescent operating point is less sensitive to changes in K_p.

Insensitivity of the MOSFET's quiescent operating point can be achieved by adding a resistor R_S into the source branch of the circuit as shown in the Fig. 2. An analysis of this new circuit, similar to before, results in the following equations:

$$V_{GG} = V_{GS} + I_D R_S \tag{3}$$

$$I_D = \frac{K_p}{2}\left(V_{GS} - V_{tr}\right)^2 = \frac{K_p}{2}\left(V_{GG} - I_D R_S - V_{tr}\right)^2 = \tag{4}$$

$$\frac{K_p}{2}\left(V_{GG} - V_{tr}\right)^2 - K_p R_S\left(V_{GG} - V_{tr}\right) I_D + \frac{K_p}{2} R_S^2 I_D^2$$

Note that Eq. (4) can be manipulated into a quadratic for drain current I_D

$$I_D^2 - \left(\frac{2\left(V_{GG} - V_{tr}\right)}{R_S} + \frac{2}{R_S^2 K_p}\right) I_D + \frac{\left(V_{GG} - V_{tr}\right)^2}{R_S^2} = 0 \tag{5}$$

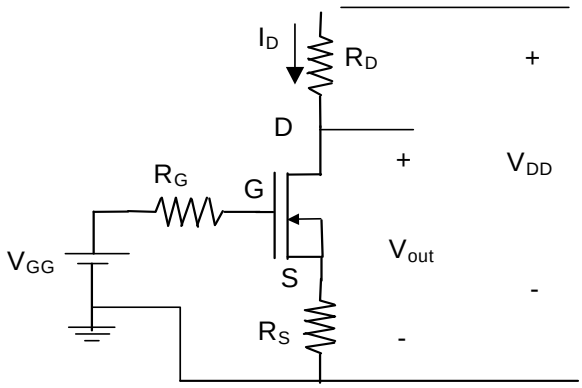

Fig. 2 Basic common source amplifier with reduced K_p sensitivity.

Notice in Eq. (5) that when R_S goes to zero (multiply through by R_S^2 and take limit as R_S go to zero), Eq. (5) simplifies to:

$$I_D = \frac{K_p}{2}\left(V_{GS} - V_{tr}\right)^2 \tag{6}$$

which is the same relationship for the circuit in Fig. 1. (Why should this be expected?) One the other hand, if the R_S is large (relative to 2), then Eq. (5) can be approximated by:

$$I_D^2 - \frac{2\left(V_{GG} - V_{tr}\right)}{R_S} I_D + \frac{\left(V_{GG} - V_{tr}\right)^2}{R_S^2} = 0 \tag{7}$$

Notice that in Eq. (5), K_p only appeared in one term, whose effect was minimized (relative to the other terms) by a large R_S value. The quadratic in Eq. (7) is a perfect square and can be rewritten as:

$$\left(I_D - \frac{\left(V_{GG} - V_{tr}\right)}{R_S}\right)^2 = 0 \qquad \text{or} \qquad I_D = \frac{\left(V_{GG} - V_{tr}\right)}{R_S} \tag{8}$$

Thus if $R_S K_p$ is large, I_D is practically independent of K_p as desired. The general solution for I_D valid for any K_p is:

$$I_D = \left(\frac{\left(V_{GG} - V_{tr}\right)}{R_S} + \frac{1}{R_S^2 K_p}\right) - \sqrt{\left(\frac{\left(V_{GG} - V_{tr}\right)}{R_S} + \frac{1}{R_S^2 K_p}\right)^2 - \frac{\left(V_{GG} - V_{tr}\right)^2}{R_S^2}} \tag{9}$$

From Eq. (9), the approximation of Eq. (8) can also be obtained by letting R_s get large (limit as R_s approaches infinity).

The circuit of Fig. 2 is still not most efficient because it requires two DC power supplies: one for V_{GG} and another for V_{DD}. The circuit in Fig. 3 remedies this. The Thévenin equivalent for the circuit consisting of V_{DD}, R_1, and R_2 in Fig. 3 gives the biasing circuit in Fig. 2 where $V_{GG} = V_{th}$ and $R_G = R_{th}$. With these Thévenin equivalents substituted into the circuit, the circuit is identical to the circuit in Fig. 2 with the exception that the bias voltage V_{GG} is now dependent on V_{DD}. The V_{GG} voltage is now controlled by the proper choice of R_1 and R_2. This eliminates the need for a separate power supply to control V_{GG}. The gate current into the MOSFET is zero so the gate voltage is thus determined by only V_{DD} and the R_1 and R_2 voltage divider.

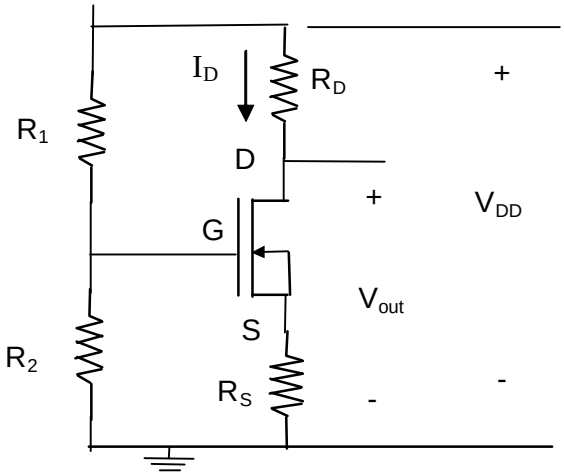

Fig. 3 Basic common source amplifier biasing with reduced K_p sensitivity and employing a single DC voltage.

The DC Operating point of this circuit is stable for two primary reasons:

- The gate voltage is determined only by the voltage divider R_1 and R_2, since insignificant current flows into the transistor gate, and is therefore independent of the transistor parameters (especially K_p).
- The source resistor R_S stabilizes the DC operating point through negative feedback. If K_p increases for any reason, such as temperature change, the subsequent rise in source current increases the voltage drop across R_S, thereby increasing V_S and thus decreasing V_{GS} (since the gate voltage V_{GG} is constant). The decrease in V_{GS} will counteract the attempted increase in I_S ($\approx I_D$).

III. Pre-Laboratory Exercise

The MOSFET you will be using in the lab is the ZVN3306A with a K_p (in SPICE) specified at 0.1233 A / V^2 (it can be as small as a third of this value) and the nominal value of the threshold voltage is $V_{tr} = 1.8$. But you have already estimated these values in Lab 2. Therefore use the values you estimated for computing the circuit parameters in

the pre-lab exercises. You are to use R_D = 1000 Ω, R_S = 470 Ω, and V_{DD}= 12 V. Note that you must use Matlab to solve some of the pre-lab problems.

Setting Transistor Quiescent Point

1. Derive the equation for the DC load line for the MOSFET circuit in Fig. 3 (with R_1, R_2 and the source resistor R_S used for added circuit stability) by relating the current I_D to the variables V_{DD}, V_{DS}, R_D, and R_S (Kirchhoff's voltage law). Be sure to sketch the circuit and the I_D vs. V_{DS} graph, which should contain sketched curves and a sketch of the load line, with end points labeled symbolically (no numbers are required on the sketch or in the equation derived above). For an example of these kind of curves see Figure 6.9 on page 323 in Horenstein.
2. Determine the quiescent operating point I_{DQ} and V_{DSQ} such that it is at the midpoint of the DC load line (to enhance the likelihood of a symmetrical output voltage swing). Determine voltage drops over R_S and R_D at this design point.
3. Write a program in Matlab to plot the DC load line superimposed with the characteristic curves (I_D versus V_{DS}) of the N-channel MOSFET for an arbitrary value of V_{GS}. Use m-files from lab lecture to help with this part. Modify your program to determine a value of V_{GS} iteratively, so the intersection of the characteristic curve and load line is close to the desired operating point. Hand in a printout of the program (with comments), a plot of the load line and characteristic curve at the determined V_{GS} value, and indicate the value of V_{GS} (you can include this value in the title of the graph or simply handwrite it on the plot with clear indication of what it is).
4. Plot the drain characteristic curves measured in Lab 2 with the load line. Does this graph suggest a similar value of V_{GS} as in the previous problem? (You will have to use a rough estimation based on an interpolation between the measured traces to determine what V_{GS} results in a trace close to your desire quiescent point). Discuss the similarities or differences in the number you obtained. Decide which is more accurate.
5. For the quiescent drain-source voltages and current computed in the previous problems, use Eq. (6) to compute the gate to source voltage (V_{GS}) at the designed quiescent operating point, and use Eq. (8) to compute the gate-to-ground voltage (V_{GG}) (same as voltage across R_2). Compare and comment on this value of V_{GS} relative to the value you found by iteration in previous problems.
6. Determine the ratio between R_1 and R_2 that will result in the V_{GG} value of the last problem and maintain this operating point. In addition, determine actual values for R_1 and R_2 that will also result in $I_{R1} = I_{DQ}/100$.

Effects of Kp Variations

7. Use the quiescent V_{GG} computed in the previous problem to compute the resulting operating point (I_{DQ} and V_{DSQ}) for the cases when K_p is 1/2 and 1/3 its design value (using Eq. (9)).

SPICE Simulation

8. Create a SPICE model for the circuit in Fig. 3 with the values given above and your computed R_1 and R_2. Use the MOSFET ZVN3306A model and change the K_p and V_{tr} values to values estimated in Lab 2. Perform a SPICE operating point analysis to

determine the voltage from the drain to the ground and the drain current. Then use SPICE operating point analysis to determine the drain source voltage (V_{DSQ}) and the drain current (I_{DQ}) when K_p has been decreased to 1/2 and 1/3 of its design value.

IV. Laboratory Exercise

1. **Measure quiescent points:** Construct the MOSFET common source amplifier (Fig. 3) using the Pre-lab values for R_1, R_2, R_S, R_D and V_{DD}. Measure the circuit's quiescent operating point by measuring V_{DSQ}, the exact value of R_D and the voltage across R_D or R_S in order to calculate I_{DQ}. Measure the quiescent operating point using the multi-meter on the DC settings. (**Discussion: Compare these values with those predicted in the pre-lab exercises**)

2. **Observe effect of increasing power supply voltage:** Increase V_{DD} to 15 V and measure the circuit's quiescent operating point as in the previous procedure. (**Discussion: How did the quiescent operating point change and how did the circuit's load line change? Is this what you would have expected? Did the circuit's quiescent operating point stay at the midpoint of the load line? Explain.**)