Phonon-energy-coupling enhancement: Strengthening the chemical bonds of the SiO_2/Si system

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We report a new effect for the SiO_2/Si system, *phonon-energy-coupling enhancement*. The vibrational modes of the Si–Si and Si–O bonds exhibit enhanced energy coupling when the rapid thermal processing (RTP) is directly applied to the SiO_2/Si system. With a combination of the RTP and deuterium (D) anneal, the strongest coupling among the Si–D, Si–Si, and Si–O bonds was observed. It is shown that not only Si–D bonds but also Si–O bonds have been strengthened dramatically when this effect is applied directly to the oxide, leading to an enhanced robustness of the oxide structure. The gate leakage current has been reduced by five orders of magnitude for thin oxides (2.2 nm) and two orders of magnitude for thick oxides (>3 nm). The breakdown voltage has been improved by ~30% © *2006 American Institute of Physics*. [DOI: 10.1063/1.2177349]

One of the fundamental limitations for scaling metal-oxide-semiconductor (MOS) transistors is that the exponential increase in gate leakage current as oxide is scaled down to below 3 nm.[1] High-*k* gate oxides have been considered as candidates to replace silicon dioxide or oxynitride.[2–4] However, there are numerous challenging issues facing high-*k* gate oxides, e.g., threshold and flat-band voltage shifts, low mobility, and Fermi-level pining at the metal-gate/oxide interface.[2–4] If the leakage current of the oxide or oxynitride can be reduced by several orders of magnitude through the structure modification, the oxide/oxynitride may be further scaled down to the ultimate limit.

In 1996, Lyding *et al.*[5] discovered the hydrogen/deuterium (H/D) isotope effect of hot-electron degradation of MOS transistors. However, the H/D isotope effect has no effect on the improvement of gate oxide.[6,7] The Si–H/D bondbreaking at the SiO_2/Si interface is determined by two competing processes. One is that the energy of the bonds is accumulated through excitation by energetic hot electrons.[8,9] The other process is de-excitation where the bond energy is taken away by coupling.[10] It was suggested theoretically that the isotope effect originates from the energy coupling from the Si–D bond to the Si–Si transverse optical (TO) phonon mode, which significantly strengthens the Si–D bonds.[10] We confirmed this theoretical prediction using Fourier transform infrared (FTIR) spectroscopy and noticed that the Si–D vibrational mode (490 cm^{-1}) does not exactly match the Si–Si TO mode (468 cm^{-1}).[11] We proposed a hypothesis that the mismatch might result in inefficient energy coupling and, if the Si–D mode could be shifted toward the Si–Si TO mode, the energy coupling might be enhanced, which might result in an enhanced H/D isotope effect. We have further tested the above hypothesis using mechanical and electrical stresses. However, no energy coupling enhancement was observed.

In this letter, we report a *surprising* discovery of phonon-energy-coupling enhancement (PECE) of the SiO_2/Si system using rapid thermal processing (RTP) directly on oxides. Its effect strengthened not only Si–D bonds but also Si–O bonds in the bulk of the oxide, leading to a large reduction of leakage current and improvement of breakdown voltage of SiO_2.

In our experiments, we used n^+ silicon wafers ($n=1\times10^{19}$ cm^{-3} and $\rho=5\times10^{-3}$ Ωcm) with (100) orientation. Because high-density electrons are present at the SiO_2/Si interface in MOS transistors, we use n^+ silicon wafers to imitate the situation. For thick oxide (>3.5 nm), thermal oxidation was performed in 100% O_2 at 900 °C. For thin oxide (<3.5 nm), thermal oxidation was performed in diluted oxygen (6% O_2) at 900 °C. Because it is unlikely to have the exact same oxide for each wafer, in order to have accurate comparison, the oxidized wafer was cut into two half-wafers. One half-wafer was used as a control sample without further processing, and the other half was subjected to RTP (Modular Process Technology Co. RTP-600S). The temperature was ramped up to 1050 °C at 27 °C/s, maintained for 1–4 min in N_2, and ramped down at 50 °C/s. Infrared absorbance spectra of the processed wafers were obtained immediately using a FTIR Spectrometer (Thermo Electron Co., Nexus 470), in conjunction with a variable angle specular reflectance accessory (Pike VeeMax II). The spectral range was selected from 400 to 900 cm^{-1}. After this, the RTP processed water was annealed in a furnace in 100% D_2 or 100% H_2 at 450 °C for 30 min, and then an infrared spectra of the sample were obtained again. The MOS capacitors were also fabricated by direct evaporation of 120 nm thick aluminium layer on top of the oxide using a shadow mask and 100 nm thick Al layer at the back of the exposed n^+ substrate. The oxide at the back of the wafer was removed in a buffered oxide etch before RTP. After RTP and before evaporation of Al, the back of the wafers were polished using a sandpaper to remove the native oxide. No chemicals were used after RTP. The MOS capacitors were annealed at 450 °C in 100% D_2 or 100% H_2 for 30 min. The oxide thickness was measured using an ellipsometer (Gaertner Sci-

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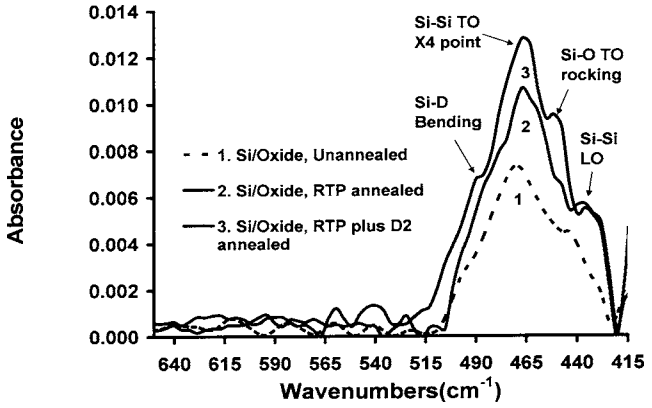

FIG. 1. FTIR spectra of Si/SiO_2 samples (23 nm oxide) based on n^+ wafers ($n=1\times10^{19}$ cm^{-3} and $\rho=5\times10^{-3}\Omega$ cm): (1) without any annealing, (2) with RTP annealing (1050 °C in nitrogen for 4 min), and (3) with RTP (1050 °C in nitrogen for 4 min) plus deuterium annealing (450 °C for 30 min.). The spectral resolution is 8 cm^{-1} with 128 scans and 65° grazing angle.

entific Co.). The current-voltage curves were measured using Agilent 4155B semiconductor analyzer. High-frequency capacitance-voltage (*C-V*) curves of MOS capacitors were measured using Keithley 590 CV analyzer.

Figure 1 shows the vibrational modes of an as-grown SiO_2/Si sample (Curve 1), a SiO_2/Si sample treated in RTP only (Curve 2), and a SiO_2/Si sample treated in RTP plus D_2 anneal (Curve 3). When the SiO_2 is subjected to RTP process only (Curve 2), the Si–Si TO phonon mode, Si–O TO rocking mode, and the Si–Si longitudinal optical (LO) mode are dramatically enhanced. It should be noted that the vibrational modes are not shifted after the RTP process, upon considering the resolution of 8 cm^{-1}. The enhancement for the Si–Si TO mode is about 50%, which is much larger than that for the D_2 anneal only (~25%).[11] When the SiO_2 is subjected to RTP plus D_2 anneal, the Si–Si TO phonon mode, Si–O TO rocking mode, and Si–D bending mode are all dramatically enhanced. The enhancement for the Si–Si TO mode is about 73% which is about three times larger than that for the D_2 anneal only (~25%).[11]

The PECE effect might involve several chemical bonds at the interface and also in the bulk of oxide and Si, including Si–D, Si–Si, and Si–O bonds. The D_2 anneal itself results in weak phonon-energy coupling among the Si–D bending mode (490 cm^{-1}), the Si–Si TO mode (468 cm^{-1}), and the Si–O TO rocking mode (448 cm^{-1}) (see Curves 2 and 3 in Fig. 1 or Ref. 11). The RTP process alone results in larger phonon-energy coupling among the Si–Si TO mode (468 cm^{-1}), the Si–O rocking mode (448 cm^{-1}), and the Si–Si LO mode (435 cm^{-1})[see Curves 1 and 2 in Fig. 1(a)]. We suggest that the thermally induced PECE effect might be caused by the change of the oxide microstructure (stress and bond-angle change) due to thermal effect.[12] The rapid cooling-down (50 °C/s) likely preserves the microstructure change of the oxide, because we did not observe the PECE effect when the SiO_2/Si sample was annealed in a furnace for slow ramp-up (0.33 °C/s) and ramp-down (~0.1 °C/s). We also observed that if the oxide is thicker than 800 Å, there is no PECE effect after the RTP process. This suggests that the PECE effect may not exist for the polycrystalline silicon/oxide stack that might have a larger tolerance for thermal shock. This also may explain why the semiconductor

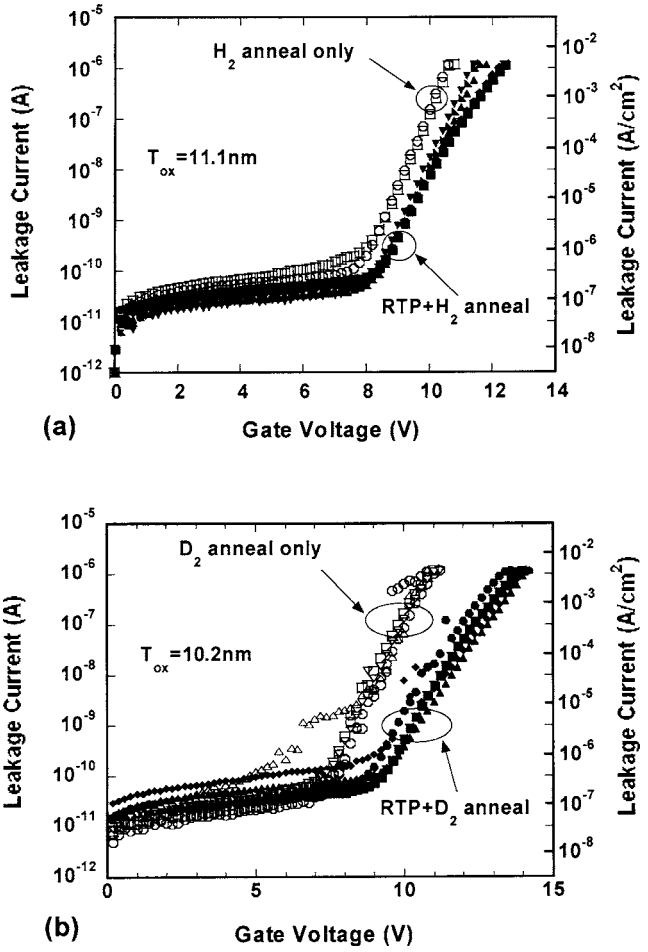

FIG. 2. Gate leakage currents of silicon MOS capacitors: (a) using oxide of 11.1 nm with hydrogen anneal (450 °C in 100% H_2 for 30 min) and with RTP (1050 °C in nitrogen for 4 min) plus hydrogen anneal (450 °C in 100% H_2 for 30 min); (b) using oxide of 10.2 nm with deuterium anneal (450 °C in 100% D_2 for 30 min) and with RTP (1050 °C in nitrogen for 4 min) plus deuterium anneal (450 °C in 100% D_2 for 30 min). The area of MOS capacitors is 4.24×10^{-4} (cm^2).

industry did not find this effect despite RTP is a routine process. It is expected that the energy of Si–D bending mode is more efficiently coupled to other modes after the RTP process, resulting in more robust Si–D bonds. Theoretically, the same argument may also be applied to the Si–O and Si–Si bonds, and thus more robust Si–O and Si–Si bonds may be expected. The direct experimental evidence for strengthening the Si–O bonds is shown in the following paragraphs.

There is no difference for leakage current between the hydrogen-annealed oxide and the deuterium-annealed oxide.[7] It is interesting to examine the effect of RTP alone on the dielectric strength of oxides. Figure 2(a) shows the leakage currents of hydrogen-annealed and RTP plus hydrogen-annealed MOS capacitors. Because the vibrational mode of Si–H bonds is far away from the range of 490–448 cm^{-1},[11] there is no energy coupling between the Si–H mode and the Si–Si TO and Si–O rocking modes. Thus, the results shown in Fig. 2(a) are exclusively from RTP. It can be seen that there is a one order-of-magnitude improvement for leakage current and 10% improvement for the breakdown voltage, resulting from RTP alone. With the combination of RTP and D_2 anneal, the leakage current and breakdown voltage are further improved, as shown in Fig. 2(b). The leakage current has been improved by two orders of magnitude and the

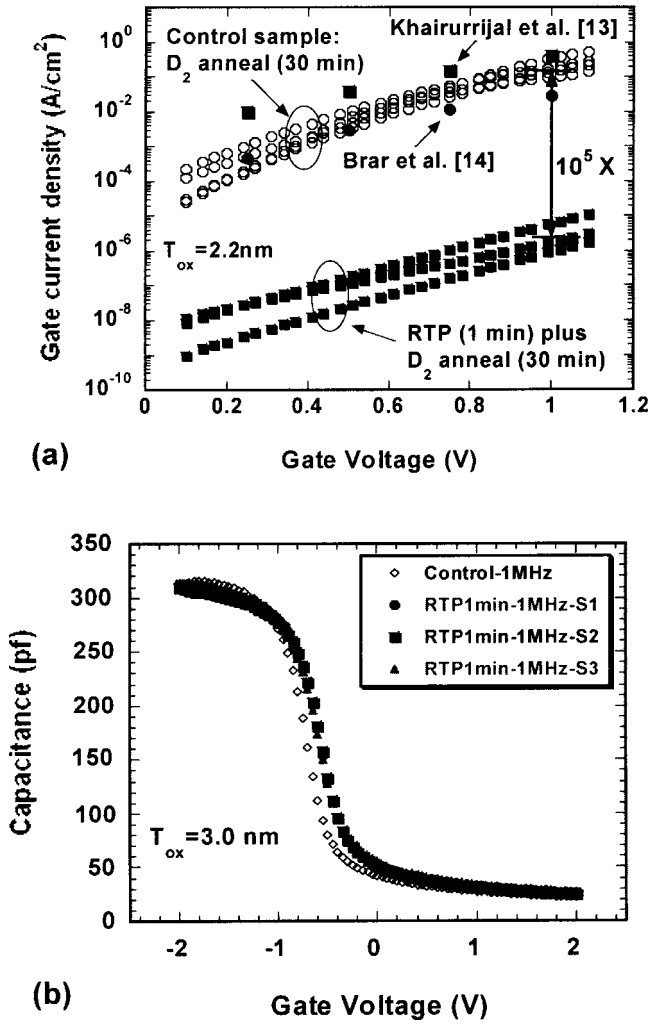

FIG. 3. Gate leakage current density of silicon MOS capacitors with oxide thickness of 2.2 nm on n^+ wafers ($n=1\times10^{19}$ cm^3) with deuterium anneal only and with RTP plus deuterium anneal. Leakage current densities of oxides reported in Refs. [13,14] are also plotted here for comparison. (b) High-frequency *C-V* curves of a control sample (without RTP) and samples after RTP with oxide thickness of 3 nm on p-Si (4×10^{15} cm^3). Both samples were finally annealed in deuterium. RTP: 1050 °C in nitrogen for 1.0 min. Deuterium anneal : 450 °C in D_2 for 30 min.

breakdown voltage has been improved by 30%. This result suggests that even if the energy of a single mode—the Si–O rocking mode—was coupled away, the Si–O bonds are significantly strengthened. The above results were obtained from thick oxides (~10 nm).]

For ultrathin oxide (<3.5 nm), the dominant leakage current comes from the direct tunneling.[13] From quantum mechanics theory, the direct tunneling current may not be affected by the strengthened Si–O bonds. However, to our great surprise, the oxide leakage current for a 2.2 nm thick oxide is reduced by five orders of magnitude after RTP anneal for 1 min plus D_2 anneal [see Fig. 3(a)]. The quality of our control samples is very similar to that reported by other groups.[13,14] It is still not clear why there is five orders-of-magnitude reduction of direct tunneling current. According to a theory proposed by Khairurrijal *et al.*[13] and refined by Stadele *et al.*,[15] electron effective mass in the oxide layer tends to increase as the oxide thickness decreases to less than 2.8 nm due to the existence of compressive stress in the oxide layer near the oxide/Si interface. Based on their theory, a plausible explanation might be that the increase in electron effective mass due to RTP-induced compress stress may further reduce the leakage current.

It is of critical importance to examine whether the dramatic leakage current reduction is due to new physics or just thickened oxides, as well as the flat-band shift due to RTP. Every time, the RTP chamber was flushed thoroughly using N_2 before processing and the oxide thickness was measured using an ellipsometer before and after RTP. We did not observe any thickness change of the oxides ranging from 1.7 to 80 nm after RTP. *C-V* measurement was also carried out to clarify this issue. Figure 3(b) shows high-frequency *C-V* curves for MOS capacitors with an oxide of 3 nm before and after RTP. It can be seen that the capacitance in accumulation was not changed after RTP, suggesting that the oxide thickness remains the same after RTP. There is a slight flat-band-voltage shift after RTP (<0.2 V), which is so small that it cannot be responsible for the large reduction of leakage currents. Therefore, it is clear that the leakage current reduction is due to the new phenomena.

From Fig. 2(b) it is clearly seen that the breakdown voltage is increased by over 30%. According to the established models,[16] energetic tunneling electrons induce defect generation, causing breakdown. With the enhanced strength of Si–O bonds, defect generation is reduced, resulting in improved breakdown voltage. Therefore, we expect that the PECE effect may not only reduce the leakage current but also enhance the reliability of ultrathin oxides/oxynitrides.

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