Nanotubes for Nanoelectronics

Zhi Chen

University of Kentucky, Lexington, Kentucky, USA

CONTENTS

1. INTRODUCTION

Carbon nanotubes (CNTs) have emerged as a viable electronic material for molecular electronic devices because of their unique physical and electrical properties [1–7]. For example, nanotubes have a lightweight and record-high elastic modulus, and they are predicted to be by far the strongest fibers that can be made. Their high strength and high flexibility are unique mechanical properties. They also have amazing electrical properties. The electronic properties depend drastically on both the diameter and the chirality of the hexagonal carbon lattice along the tube [8–10].

Carbon nanotubes were discovered by Iijima in 1991 at the NEC Fundamental Research Laboratory in Tsukuba, Japan [1]. Using a transmission electron microscope (TEM), he found carbon tubes consisting of multiple shells (see Fig. 1). These early carbon tubes are called multiwall nanotubes (MWNTs). Since then, extensive research has been focused on synthesis and characterization of carbon nanotubes. In 1993, Ijima's group [11] and Bethune et al. [12] at IBM Almaden Research Center at San Jose, California, synthesized carbon nanotubes with a single shell, called single-wall nanotubes (SWNTs). Because of their simple and well-defined structure [13], the single-wall nanotubes serve

as model systems for theoretical calculations and for critical experimental studies. Since then, the physical and electrical properties of carbon nanotubes have been studied extensively. Only a few years ago, people began to utilize carbon nanotubes' unique electrical properties for electron device applications. Up to now, there has been no extensive review to cover the progress in nanoelectronic devices using carbon nanotubes.

In this chapter, I aim to present extensive review on progress in electronic structure and transport properties of carbon nanotubes and nanoelectronic devices based on carbon nanotubes ranging from quantum transport to field-effect transistors. This chapter is organized as follows. It begins with brief review of the progress in micro- and nanoelectronic devices prior to carbon nanotubes (Section 2). Then the synthesis and physical properties of carbon nanotubes will be discussed in Section 3. Nanoelectronic devices based on carbon nanotubes including single-electron transistors (SETs), field-effect transistors, logic gates, and memory devices will be reviewed in Sections 4 and 5. The chemical doping, junctions, and metal–nanotube contacts will be described in Section 6. Finally, nanofabrication based on carbon nanotubes including controlled growth and selective placement of nanotubes on patterned Si substrates will be reviewed in Section 7. Since the discovery of carbon nanotubes, over 1000 papers on carbon nanotubes have been published. It is unlikely that every paper will be included in this chapter, because most papers dealt with synthesis, physical, and chemical properties of nanotubes. In this chapter, I will focus on electrical properties of nanotubes, nanoelectronic devices constructed with nanotubes, and nanotube-based nanofabrication.

2. PROGRESS IN NANOELECTRONICS PRIOR TO NANOTUBES

In 1959 Richard Feynman delivered his famous lecture, "There is Plenty of Room at the Bottom." He presented a vision of exciting new discoveries if one could fabricate materials and devices at the atomic and molecular scale. It was not until 1980s that instruments such as scanning tunneling microscopes (STM), atomic force microscopes (AFM), and near-field microscopes were invented. These instruments
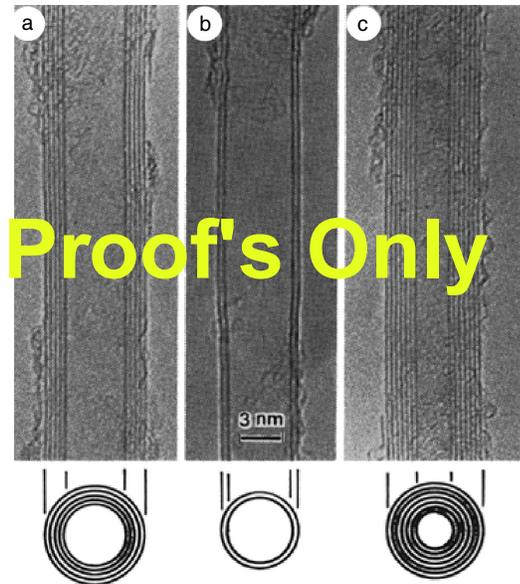
Figure 1. Cross-section images of carbon nanotubes by a high-resolution TEM. Reprinted with permission from [1], S. Iijima, *Nature* 354, 56 (1991). © 1991, Macmillan Publishers Ltd.

provide "eyes" and "fingers" required for nanostructure measurement and manipulation [14]. The driving force for nanoelectronics is the scaling of microelectronic devices to nanoscale, which is the engine for modern information revolution. The microelectronics revolution began in 1947 when John Bardeen, Walter H. Brattain, and William Shockley of Bell Telephone Laboratories invented the first solid state transistor, the Ge point-contact transistor [15]. Solid state transistors had far superior performance, much lower power consumption, and much smaller size than vacuum triodes. People began to produce individual solid state components to replace the vacuum tubes in circuits in a few years after the invention. In 1958, Jack Kilby of Texas Instruments conceived a concept for fabrication of the entire circuit including components and interconnect wires on a single silicon substrate [16]. In 1959, Robert Noyce of Fairchild Semiconductor individually conceived a similar idea [15]. This concept has evolved into today's very-large-scale integrated circuits or "microchips," which consist of millions of transistors and interconnect wires on a single silicon substrate. The major driving force for this revolutionary progress is miniaturization of transistors and wires from tens of micrometers in the 1960s to today's tens of nanometers. The scaling down of transistor and interconnect wires led to more and more transistors being incorporated into a single silicon chip, resulting in faster and more powerful computer chips. With the success in microelectronics and of the semiconductor industry, it is natural to consider extending the micrometer size devices to nanometer size devices.

2.1. STM/AFM-Based Nanofabrication

There was not much progress in nanoelectronics until the 1980s. In 1981, the scanning tunneling microscope, invented by G. K. Binnig and H. Rohrer of IBM Zurich Research Laboratory, produced the first images of individual atoms on the surfaces of materials [17]. Later the STM was used to modify surfaces at the nanometer scale and the manipulation and positioning of single atoms on surface was achieved [18]. In 1993, Crommie et al. [19] eloquently demonstrated with a "quantum corral" where the STM can be used not only to characterize the electronic structure of materials on a truly quantum scale, but also to modify this quantum structure. This suggested that the STM and AFM might be used for atom-by-atom control of materials modification, leading to atomic resolution. This potential motivated researchers to attempt to use STM and AFM for nanolithography [20–25]. This task has not been easy due to the irreproducibility of the modifications, the slow "write" speed, and the difficulty of transferring such fine manipulations into functioning semiconductor devices [21]. Until now, reliable fabrication and robust pattern transfer for linewidths below 10 nm has not been achieved yet.

2.2. Metal-Oxide-Semiconductor Field-Effect Transistors

As early as the 1920s and 1930s, a concept for amplifying devices based on the so-called *field effect* was proposed with little understanding of the physical phenomena [26, 27]. After 30 years, the field-effect transistor based on the SiO_2/Si structure finally became practical [28]. Since that time, the metal-oxide-semiconductor field-effect transistor (MOSFET) has been incorporated into integrated circuits and has grown to be the most important device in the semiconductor industry ranging from memory chips, microprocessors, and many other communication chips. Figure 2a shows the structure of an *n*-channel MOSFET. It consists of *p*-type Si, heavily doped n^+ source and drain, and an insulated gate. When the gate voltage is zero, the region underneath the gate oxide is *p*-type. There are two pn^+ junctions near the source and the drain. When applying a voltage across the source and the drain, either of the two pn^+ junctions is reverse biased. Thus the transistor conducts no current. When the gate voltage is larger than zero but less than its threshold voltage, depletion happens underneath the gate oxide, which is still not conductive. When the gate voltage is larger than its threshold voltage, an inversion layer (*n*-type) is induced underneath the gate oxide, which forms a conduction channel connecting both source and drain. Thus the transistor conducts current. The typical I–V curves for an *n*-MOSFET with a gate length of 0.25 μm and a width of 15 μm are shown in Figure 2b. The driving force behind this
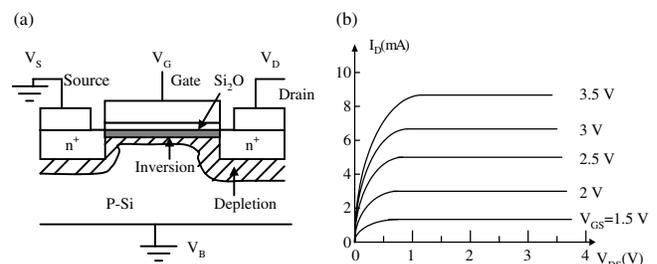

Figure 2. (a) Schematic structure of a Si MOSFET used in various microchips for digital signal processing and (b) its current–voltage characteristics.

remarkable development is the cost reduction and performance enhancement of integrated circuits (ICs) due to the continuous miniaturization of transistors and interconnect wires. The continuous scaling of transistors and the increase in wafer size has been and will continue to be the trend for the semiconductor industry. The transistor gate length (feature size) has been dramatically reduced for the past three decades [29, 30]. The lateral feature size or linewidth of a transistor has been shrunk by almost 50 times from about 10 μm to the 100 nm range, allowing over 10,000 times more transistors to be integrated on a single chip. Microprocessors have evolved from their 0.1 MHz ancestors used for watches and calculators in the early 1970s to the current 2 GHz engines for personal computers. Memories have grown from 1-Kb pioneers used almost exclusively for mass storage in central computers to the 128/256-Mb dynamic random access memory commonly used in personal computers today. Most advanced chips on the market now have feature sizes of 100 nm. According to the Semiconductor Industry Association's *International Technology Roadmap for Semiconductors* [31], the feature sizes for lithography were projected as follows: *130 nm in 2001, 100 nm in 2003, 80 nm in 2005, 35 nm in 2007, 45 nm in 2010, 32 nm in 2013, and 22 nm in 2016*. The wafer size has increased from 2 inches in the early 1970s to the current 12 inches. Therefore, the performance of ICs has been dramatically improved, and the cost for manufacturing has been dramatically reduced. However, the device scaling is approaching its limit. It was suggested that MOS device scaling might not be extended to below 10 nm because of physical limits such as power dissipation caused by leakage current through tunneling [32–34]. In addition, once electronic devices approach the nano- and molecular scale, the bulk properties of solids are replaced by the quantum-mechanic properties of a relatively few atoms such as energy quantization and tunneling. It is therefore important to search for alternative devices for Si MOS devices.

2.3. Quantum-Effect Devices

In order for a transistor-like device to operate on the nano- and molecular scale, it would be advantageous if it operated based on quantum mechanical effects. Even though the study of single-electron charging effects with granular metallic systems dates back to the 1950s [35, 36], it was the research of Likharev in 1988 that laid much of the groundwork for understanding single-charge transport in nanoscale tunnel junctions [37, 38]. When a small conductor (island) is initially neutral, it does not generate any appreciable electric field beyond its border. In this state, a weak external force (due to electric field) may bring in an additional electron from outside. The net charge in the island is $(-e)$ and the resulting electric field repulses the following electrons which might be added. In order to have an electron to be added it needs to overcome the charging energy and its kinetic energy. Thus, the electron additional energy E_a is given by

$$E_a = E_c + E_k$$

Here E_c is the charging energy that is given by

$$E_c = \frac{e^2}{C}$$

where e is the charge of electron and C is the capacitance of the conductive island. The kinetic energy is expressed as

$$E_k = \frac{1}{g(\varepsilon_F)V}$$

where $g(\varepsilon_F)$ is the density of states on the Fermi surface and V is the volume of the island.

For the island diameter > 2 nm, $E_c \gg E_k$. Thus

$$E_a \approx E_c = \frac{e^2}{2C}$$

For the 100 nm-scale island, E_a is of the order of 1 meV, corresponding to ~10 K in temperature. If the island size is reduced to below 10 nm, E_a approaches 100 meV, and some single-electron effects become visible at room temperature.

Among quantum-effect devices, single-electron transistors have been most extensively studied [38–40]. The basic structure of a SET is shown in Figure 3a. An island or quantum dot is placed between two electrodes (source and drain) with the third electrode (gate) is placed by its side. When a voltage is applied, an electron tunnels onto the island and the charging energy is increased by $E_a \approx e^2/2C$ and this increase acts as a barrier to the transfer of any further electrons. At small source–drain voltage, there is no current. The *I–V* characteristic is shown in Figure 3b. The current is blocked from $-V_c$ to V_c, called *Coulomb blockade*. When the source–drain voltage is increased and reaches a level greater than V_c, where the energy barrier is eliminated, electrons can cross the island and the current increases with the applied voltage. The threshold voltage V_c is a periodical function of gate voltage.

Coulomb charging effects were originally observed in metallic film by Gorter in 1951 [35]. The first successful metallic single-electron transistor was made by Fulton and Dolan in 1987 [36]. They used a relatively simple technique in which two layers of aluminum were evaporated *in-situ* from two angles through the same suspended mask formed by direct e-beam writing. Since then, single-electron transistors have been demonstrated in numerous experiments using a wide variety of device geometry, materials, and techniques. SETs based on metallic nanodots were fabricated. Chen et al. [41] reported that SETs with metal dots of 20–30 nm and gaps of 20–30 nm were fabricated by ionized beam evaporation. The electrical results showed clear Coulomb blockade at temperature as high as 77 K. Novel lateral metallic SETs can be based on gold colloidal particles. These particles are very uniform in size and can be obtained in a range
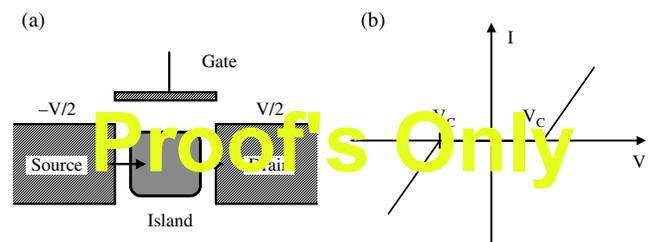

Figure 3. (a) Schematic structure of a capacitively coupled single-electron transistors and (b) its source–drain dc *I–V* curves.

of sizes. The devices can be fabricated by placing the particles in the gap between the source and drain. Klein et al. [42] obtained the Coulomb blockade characteristics based on gold colloidal particles at 77 K. Nakamura et al. [43] fabricated Al-based SETs, which operated at 100 K. Shirakashi et al. [44] fabricated Nb/Nb oxide-based SETs at room temperature ($T = 298$ K). The further reduction of the tunnel junction is performed by scanning probe microscope (SPM)-based anodic oxidation. The Coulomb blockade characteristics were clearly shown at room temperature.

Single-electron effects have also been observed in a number of semiconductor based structures. The first device was realized by squeezing the two-dimensional electron gas (2DEG) formed at the AlGaAs/GaAs heterostructure [45]. It consists of a pattern of metal gates evaporated onto the semiconductor surface. The voltages were applied to the gates to squeeze the 2DEG so that islands and tunnel barriers were formed. Coulomb blockade can be observed if the regions are sufficiently squeezed. Coulomb blockade effects have also been demonstrated on silicon based devices. A number of experiments have been reported on structures based on silicon-on-insulator (SOI). This is particularly important because silicon processing technology is the mainstream technology in the semiconductor industry. The silicon based SET technology can be easily integrated into the mainstream technology once it is successful. Ali and Ahmed [46] showed the first SOI-based SETs with clear Coulomb blockade. Leobandung et al. [47] also demonstrated silicon quantum-dot transistors with a 40-nm dot. The Coulomb blockade was clearly seen at temperature of 100 K. Takahashi et al. [48] and Kurihara et al. [49] scaled the silicon-based SETs to make significantly smaller islands and obtained Coulomb oscillation at temperatures approaching room temperature. Zhuang et al. [50] reported fabrication of silicon quantum-dot transistors with a dot of ~12 nm with a clear Coulomb blockade at 300 K. Guo et al. [51] successfully fabricated a silicon single-electron transistor memory, which operated at room temperature. The memory is a floating gate MOS transistor in silicon with a channel width (~10 nm) smaller than the Debye screening length of a single electron and a nanoscale polysilicon dot (7 nm × 7 nm) as the floating gate embedded between the channel and the control gate. Storing one electron on the floating gate screens the entire channel from the potential on the control gate and leads to a discrete shift in the threshold voltage, a staircase relation between the charging voltage and the shift. SETs based on Si nanowires have also been demonstrated [52]. It was shown that quantum wires with a large length to width ratio show clear Coulomb oscillations at temperatures up to 77 K.

3. SYNTHESIS AND ELECTRICAL PROPERTIES OF CARBON NANOTUBES

3.1. Synthesis of Carbon Nanotubes

Although this chapter focuses on nanoelectronic devices, I still cover some of synthesis methods and approaches which may be helpful for interested readers. It should be pointed out that I am unable to include all the papers in synthesis because extensive research has been conducted for growth of carbon nanotubes.

Although multiwall carbon nanotubes were discovered in 1991 by Iijima, it is quite likely that such MWNTs were produced as early as the 1970s during research on carbon fibers [2]. The multiwall carbon nanotubes discovered in 1991 were obtained from the fullerene soot produced in an arc discharge [1]. As early as in 1986, Saito of the University of Kentucky studied the soot produced by a candle-like methane flame. A quartz fiber was inserted into the flame from the side and left there for a certain period of time [53]. When the fiber was raised to a certain height, a smooth film was coated on the fiber surface, which appeared to be brown in color. With increase of the sampling height beyond the critical height, the color of the deposited material changed from brown to black, and its surface appearance also changed from smooth to a rough and bumpy structure. The SEM analysis identified the rough surface material to be soot and the initial light brown material from the methane flame to be polyhedral-shaped crystal-like particles [54]. The deposit from the acetylene flame had a spider-web shape of entangled, long, narrow diameter strings, of which the detailed structure remained unknown until recent TEM study [55]. It was a surprise that the recent TEM study showed that the entangled long strings synthesized in 1986 are *carbon nanotubes*, which were discovered later by Iijima in 1991. Recently Saito's group repeated his 1986 experiments and synthesized CNTs using methane flames [56] and ethylene flames [57]. In 1993, Iijima and Ichihashi [11] synthesized single-wall carbon nanotubes of 1-nm diameter. Bethune and co-workers [12] also, at the same time, synthesized single-wall carbon nanotubes using cobalt catalyst. The research on carbon nanotubes really took off when Smalley and co-workers at Rice University found a laser ablation technique that could produce single-wall carbon nanotubes at yields up to 80% instead of the few percent yields of early experiments [58–60]. Kong and co-workers [61] at Stanford University used a chemical vapor deposition (CVD) technique to grow carbon nanotubes by decomposing an organic gas over a substrate covered with metal catalyst particles. The CVD approach has the potential for making possible large-scale production of nanotubes and growth of nanotubes at specific sites on patterned Si substrates [62, 63].

3.2. Electronic Structures of Carbon Nanotubes

Just in one year after the discovery of carbon nanotubes, their electronic structures were theoretically studied based on local-density-functional calculation [8], tight-binding band-structure calculation [9, 10, 64]. Figure 4a shows how to construct a carbon nanotube by wrapping up a single sheet of graphite such that two equivalent sites of the hexagonal lattice coincide; that is, point C coincides with the origin (0, 0) [65]. The wrapping vector **C**, which defines the relative location of the two sites, is specified by a pair of integers (n, m) that relate **C** to the two unit vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ ($\mathbf{C} = n\mathbf{a}_1 + m\mathbf{a}_2$). A tube is called "armchair" if n equals m, and "zigzag" in the case $m = 0$. All other tubes are of the "chiral" type with a finite wrapping angle

(A)

(B)

no. 10

Proof's Only
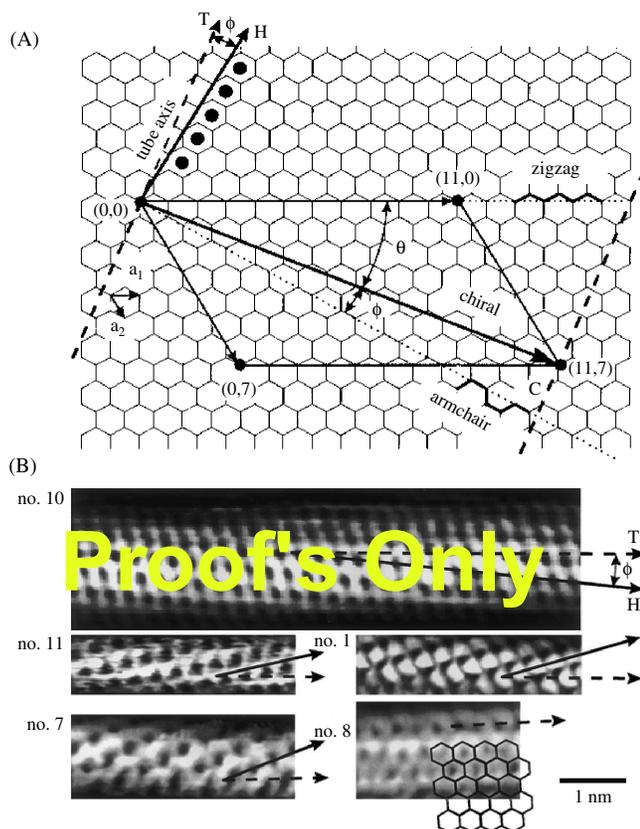
no. 11   no. 1

no. 7   no. 8

1 nm

Figure 4. Relation between the hexagonal carbon lattice and the chirality of carbon nanotubes. (A) Construction of a carbon nanotube from a single graphene sheet by rolling up the sheet along the wrapping vector C. (B) Atomically resolved STM images of individually single-wall carbon nanotubes showing chirality. Reprinted with permission from [65], J. W. G. Wildoer et al., *Nature* 391, 59 (1998). © 1998, Macmillan Publishers Ltd.

ϕ ($0° < \phi < 30°$). Figure 4b shows the STM images of single-wall carbon nanotubes [65]. Tube 10 has a chiral angle $\phi = 7°$ and a diameter $d = 1.3$ nm, which corresponds to the (11, 7) type of panel A. The dependence of the electronic structure of nanotubes on the tube indices (n, m) can be understood by taking the two-dimensional graphene sheet as a starting point. In the circumferential direction (along **C**), the periodic boundary conditions $\mathbf{C} \cdot \mathbf{k} = 2\pi q$ can be applied, where **k** is the wave vector and q is an integer. This leads to a set of allowed values for k, which can be substituted into the dispersion relations for the tube, with q representing the various modes. Electronic energy band structure calculations [3, 8–10, 64] predicted that armchair ($n = m$) tubes behave like metallic. For all other tubes (chiral and zigzag) there exist two possibilities. If $(n - m)/3$ is an integer, tubes are expected to be metallic, and if $(n - m)/3$ is not an integer, tubes are predicted to be semiconducting with an energy gap depending on the diameter. The energy gap can be expressed as $E_{\text{gap}} = 2\gamma_0 a_{\text{C−C}}/d$, where γ_0 is the C–C tight-binding overlap energy, $a_{\text{C−C}}$ is the nearest neighbor C–C distance (0.142 nm), and d is the diameter. Figure 5 shows the calculated energy band structure of zigzag nanotubes (12, 0) in (c) and (13, 0) in (d). [The geometric structure of the tubes and the first Brillouin zone of a graphene sheet are
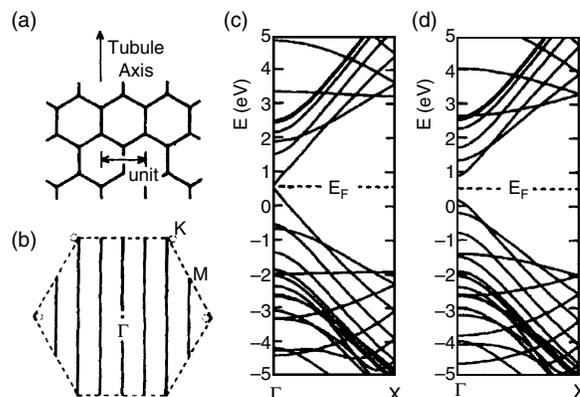

Figure 5. (a) The geometric configuration for a single-wall carbon nanotube $(n, 0)$. (b) The first Brilluoin zone of a graphite sheet and the wave vector allowed by the periodic boundary condition along the circumference for $n = 6$ (solid lines). Band structures of (c) (12,0) and (d) (13,0) single-wall nanotubes. Reprinted with permission from [9], N. Hamada et al., *Phys. Rev. Lett.* 68, 1579 (1992). © 1992, American Physical Society.

shown in (a) and (b).] The tube (12,0) is metallic, satisfying the condition of $(n - m)/3$ being integer; and the tube (13,0) is semiconducting with an energy gap of 0.697 eV, which falls into the category of $(n - m)/3$ being noninteger. Figure 6 shows the calculated energy band gaps of tubes $(n, 0)$ with $n = 6–15$. For $n = 6, 9, 12, 15$ [i.e., $(n - m)/3$ is integer], energy gaps are almost zero, and for $n = 7, 8, 10, 11, 13, 14$, [i.e. $(n - m)/3$ is noninteger], the energy gaps are ranging from 0.6 to 1.2 eV. Figure 7 shows the calculated one-dimensional (1D) electronic density of states for (a) a (9,0) nanotube and (b) a (10,0) nanotube [66]. The 1D density of state (DOS) of both nanotubes shows a series of spikes. Each spike corresponds to the energy threshold for an electronic subband caused by the quantum confinement of electrons in the radial and circumferential directions of nanotubes. The (9,0) nanotube is metallic and the (10,0) tube is semiconducting.

Experimental measurements [65, 67] of the energy bands of nanotubes confirmed these theoretical calculations. Figure 8a shows a selection of I–V curves obtained by scanning tunneling spectroscopy (STS) on different tubes [65]. Most curves show a low conductance at low bias, followed by several kinks at larger bias voltages. Figure 8b shows
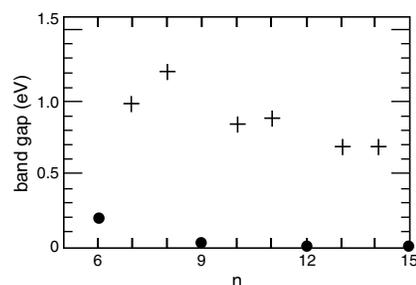

Figure 6. The energy bandgap as a function of the number of hexagons on the circumference for a single-wall nanotube $(n, 0)$. Reprinted with permission from [9], N. Hamada et al., *Phys. Rev. Lett.* 68, 1579 (1992). © 1992, American Physical Society.
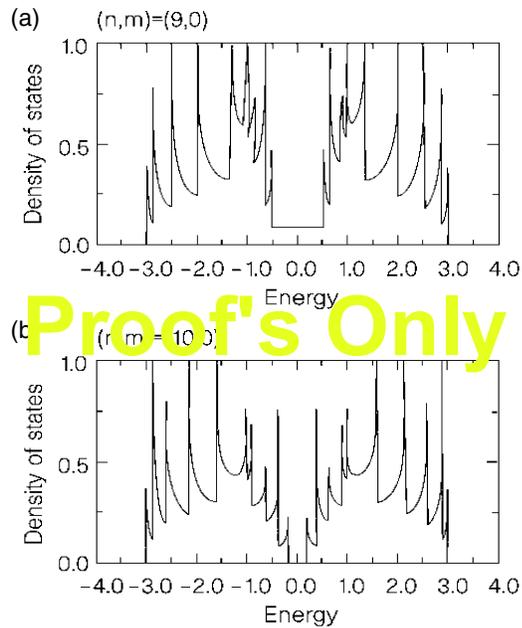
Figure 7. Calculated one-dimensional electronic density of states for (a) a (9,0) nanotube and (b) a (10,0) nanotube. Reprinted with permission from [66], M. S. Dresshaus, *Nature* 391, 19 (1998). © 1998, Macmillan Publishers Ltd.
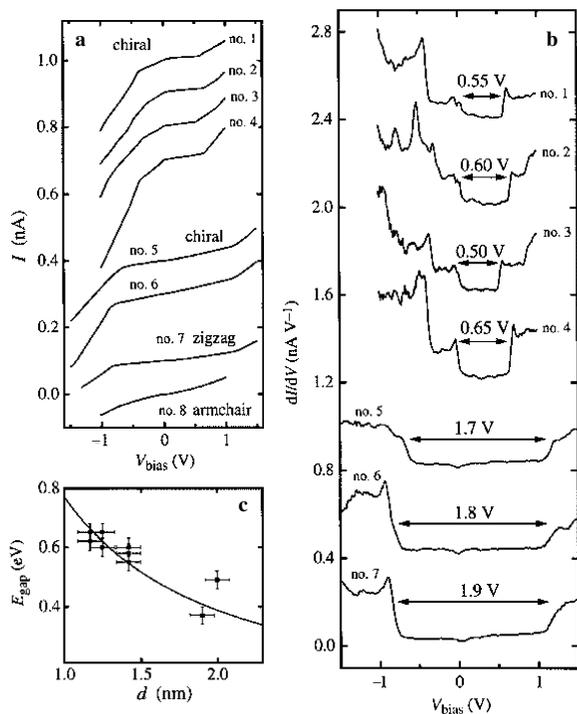

Figure 8. (a) Current–voltage curves obtained by tunneling spectroscopy on various nanotubes. (b) The derivatives dI/dV show two groups: a semiconducting one with gap values around 0.5–0.6 eV and a metallic one with gap values around 1.7–1.9 eV. (c) Energy gap versus diameter of semiconducting chiral tubes. Reprinted with permission from [65], J. W. G. Wildoer et al., *Nature* 391, 59 (1998). © 1998, Macmillan Publishers Ltd.

the dI/dV curves. There are two categories: the one has a well-defined gap values around 0.5–0.6 eV and the other has significantly larger gap values of ∼1.7–2.0 eV [65]. The gap value of the first category agrees very well with the predicted gap values for semiconducting tubes. As shown in Figure 9c, the energy gap decreases as the tube diameter d increases. This also agrees well with theoretical gap values obtained for an overlap energy $\gamma_0 = 2.7 \pm 0.1$ eV, which is close to the value $\gamma_0 = 2.5$ eV suggested for a single graphene sheet [3]. The very large bandgaps observed for the second category of tubes, 1.7–2.0 eV, are in good agreement with the values of 1.6–1.9 eV obtained from one-dimensional dispersion relations for a number of metallic tubes with $(n - m)/3$ being integer [65]. These metallic nanotubes are expected to have a small but finite DOS near the Fermi energy (E_F) and the apparent "gap" is associated with DOS peaks at the band edges of the next one-dimensional modes. Sharp van Hove singularities in the DOS are predicted at the onsets of the subsequent energy bands, reflecting the one-dimensional character of carbon nanotubes (see Fig. 7). The derivative spectra indeed show a number of peak structures (Fig. 8b). For semiconductors, it has been argued that $(dI/dV)/(I/V)$ represents the DOS better than the direct derivative dI/dV, partly because the normalization accounts for the voltage dependence of the tunnel barrier at high bias [68, 69]. In Figure 9, $(dI/dV)/(I/V)$ is shown, where sharp peaks are observed, resembling that predicted for van Hove singularities. The experimental peaks have a finite height and are broadened because of hybridization of wave functions. Raman scattering experiments also support the one-dimensional subband of nanotubes [70, 71]. Resistivity measurements of armchair SWNTs also suggested their metallic behavior, consistent with the theoretical calculation [72, 73]. In addition, momentum-dependent high-resolution electron energy-loss spectroscopy was performed on purified SWNTs [74]. Two groups of excitations have been found.
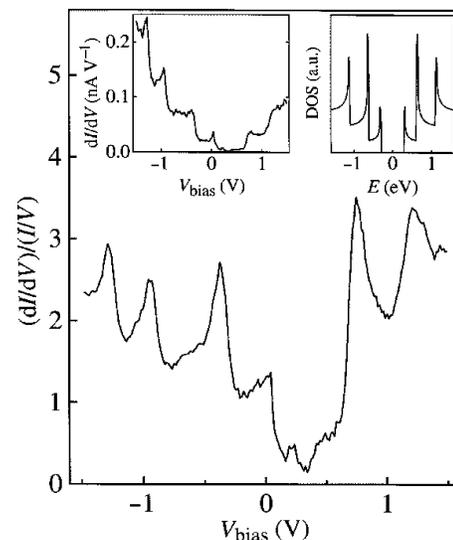

Figure 9. *(dI/dV)/(I/V)* which is a measure of the density of states versus V for nanotube 9. The left inset displays the raw dI/dV data, and the right inset is the calculated DOS. Reprinted with permission from [65], J. W. G. Wildoer et al., *Nature* 391, 59 (1998). © 1998, Macmillan Publishers Ltd.

One group is nondispersive and the energy position is characteristic of the separation of the van Hove singularities in the electronic DOS of the different types of nanotubes. The other one shows considerable dispersion and is related to a collective excitation of the π-electron system [74].

As pointed out by Dresselhaus [66], these results [66, 67] showed a wide range of helicities for SWNTs which contradict the narrow distribution of chiral angles determined by Raman scattering experiments [71] carried out on SWNT ropes synthesized by the same technique. In addition, van Hove singularities (energy threshold for an electronic subband) were also clearly resolved [65] in the experimental DOS of both chiral and achiral nanotubes. The observation of these well-separated and clearly resolved sharp spikes in the DOS of SWNTs with chiral symmetry was not expected [66]. Further calculation of the $\sigma + \pi$ electron densities of states of chiral carbon nanotubes using a tight-binding Hamiltonian showed that the electronic structures of SWNTs with chiral symmetry are similar to the zigzag and armchair ones [73, 74]. Fluorescence has also been observed directly across the bandgap of semiconducting carbon nanotubes, supporting the theoretical calculation of energy band structure of carbon nanotubes [77]. Most SWNTs synthesized using the current technologies are ropes consisting of many individual SWNTs. The first-principle calculation of electronic band structure of close-packing of individual nanotubes (10,10) into a rope showed that a broken symmetry of the (10,10) tube caused by interactions between tubes in a rope induces a pseudogap of about 0.1 eV at the Fermi level [78]. This pseudogap strongly modifies many of the fundamental electronic properties of carbon nanotube ropes. Structures of molecular electronic devices ultimately depend on tuning the interactions between individual electronic states and controlling the detailed spatial structure of the electronic wave functions in the constituent molecules. It is amazing that the two-dimensional images of electronic wave functions in metallic SWNTs have been obtained using STS [79]. These measurements reveal spatial patterns that can be directly understood from the electronic structure of a single graphite sheet. This represents an elegant illustration of Bloch's theorem at the level of individual wave functions.

3.3. Quantum Transport of Carbon Nanotubes

The electrical transport experiments on individual tubes are highly preferred. The first measurements on individual nanotubes were carried out on MWNTs [80–84]. Langer et al. [82] reported on electrical resistance measurements of an individual MWNT down to a temperature of $T = 20$ mK. The conductance exhibited a $\ln T$ dependence and saturated at low temperature. A magnetic field applied perpendicular to the tube axis increased the conductance and produced aperiodic fluctuations. Their data also support two-dimensional weak localization and universal conductance fluctuations in mesoscopic conductors. These early studies on MWNTs suggested defect scattering, diffusive electron motion, and localization with a characteristic length scale of only a few nanometers. In addition, the electrical properties of individual MWNTs have been shown to vary strongly from tube to tube.

3.3.1. Ballistic Transport

It came as a surprise when the first experiments on individual SWNTs showed that nanotubes could have delocalized wave functions and behave as true *quantum wires* [85, 86]. Electrical measurement indicates that conduction occurs through well separated, discrete electronic states that are quantum-mechanically coherent over long distance, at least >140 nm [86]. Theory predicts that the electrons flow ballistically through carbon nanotubes and that the conductance is quantized [87–90]. Quantized conductance results from the electronic waveguide properties of extremely fine wires and constrictions. When the length of the nanotube is less than the mean-free path of electrons, the electronic transport is ballistic (i.e., each transverse waveguide mode or conduction channel contributes $G_0 = 2e^2/h$ to the total conductance). Theoretical calculation indicates that conducting single shell nanotubes have two modes or two conduction channels [87–90]; this predicts that the conductance of a single-walled nanotube is $2G_0$ independent of diameter and length. Another important aspect of ballistic transport is that no energy is dissipated in the conductor and the Joule heat is dissipated at the contacts of metal and nanotubes. Conductance measurements on MWNTs revealed that only one conduction channel G_0 exists in MWNTs, which conduct current ballistically over a length of 4 micrometers [91]. Recently, quantized conductance has been observed in SWNTs [92], which has two conduction channels $2G_0$, in agreement with the theoretical calculation. Theoretical studies also suggests that conduction electrons in armchair nanotubes experience an effective disorder averaged over the tube's circumference, leading to electron-mean-free paths that increase with nanotube diameter [93]. This increase should result in exceptional ballistic transport properties and localization lengths of 10 μm. For (10,10) armchair nanotubes, the mean-free path of 7.5 μm is obtained [93].

The fundamental reason for ballistic transport of carbon nanotubes is their *perfect* symmetric and periodic structure. It was shown that defects introduced into the nanotubes serve as scattering centers [94], which destroys the perfect structure. Theoretical calculation also showed that the absence of backscattering was demonstrated for single impurity with long range potential in metallic tubes [95–97] and a stepwise reduction of the conductance was inferred from multiple scattering on a few lattice impurities [98, 99]. Therefore, chemically doped semiconducting SWNTs may behave as diffusive conductors with shorter mean-free paths. It has been reported experimentally that mean-free paths of SWNTs are lower than the ones of reported structurally equivalent metallic SWNTs [100]. The backscattering contribution to the conductivity has been demonstrated to be more significant for doped semiconducting systems [101].

3.3.2. Other Transport Properties

Zeeman Effect Tans et al. [86, 102] observed an excited state by applying a magnetic field perpendicular to the tube axis, which moved relative to the ground state at a rate corresponding to a *g*-factor of 2.0 ± 0.5, consistent with the expected free-electron Zeeman shift. Cobden et al. [103] later studied the spin state by applying a magnetic field along the tube axis of the nanotube rope. It is concluded that as

successive electrons are added, the ground state spin oscillates between S_0 and $S_0 + \frac{1}{2}$, where S_0 is most likely zero. This results in the even/odd nature of the Coulomb peaks, which is also manifested in the asymmetry of the current–voltage characteristics and the peak height [106]. It is suggested that the g-factor of the Zeeman split is 2.04 ± 0.05 [104].

Aharonov–Bohm Effect When electrons pass through a cylindrical electrical conductor aligned in the magnetic field, their wavelike nature manifests itself as a periodic oscillation in the electrical resistance as a function of the enclosed magnetic flux. This phenomenon reflects the dependence of the phase of the electron wave on the magnetic field known as the Aharonov–Bohm effect [105], which causes a phase difference, and hence interference, between partial waves encircling the conductor in opposite directions. Theoretical studies showed [86, 106] that upon applying a magnetic field along the tube axis, the electronic structure of a carbon nanotube drastically changes from a metal to a semiconductor or from a semiconductor to a metal during variation of magnetic flux ϕ. The energy dispersion without the spin-***B*** interaction is periodic in ϕ, with a period ϕ_0, as a result of the Aharonov–Bohm effect. Magnetoresistance measurements were carried out on individual MWNTs, which exhibit pronounced resistance oscillations as a function of magnetic flux [107]. The oscillations are in good agreement with theoretical predications for the Aharonov–Bohm effect in a hollow conductor with a diameter equal to that of the outermost shell of the nanotubes. Significant electron–electron correlation has been observed in experiments [108]. Electrons entering the nanotube in a low magnetic field are observed to have all the same spin direction, indicating spin polarization of the nanotube. When the number of electrons is fixed, variation of an applied gate voltage can significantly change the electronic spectrum of the nanotube and can induce spin-flips [108].

Luttinger Liquid Electron transport in conductors is usually well described by Fermi-liquid theory, which assumes that energy states of electrons near the Fermi level E_F are not qualitatively altered by Coulomb interactions. In one-dimensional systems, however, even weak Coulomb interactions cause strong perturbations. The resulting system, known as Luttinger liquid, is predicted to be distinctly different from its two- or three-dimensional counterpart [109]. Coulomb interactions have been studied theoretically for SWNTs [110, 111] and MWNTs [112]. Long-range Coulomb forces convert an isolated (N, N) armchair carbon nanotube into a strong renormalized Luttinger liquid [110]. At high temperatures, anomalous temperature dependence for the interaction, resistivity due to impurities, and power-law dependence for the local tunneling density of states were found. At low temperatures, the nanotube exhibits spin-charge separation, signaling a departure from orthodox theory of Coulomb blockade. Experimental measurements of the conductance of bundles ("ropes") of SWNTs as a function of temperature and voltage confirmed these theoretical studies [113].

4. SINGLE-ELECTRON TRANSISTORS

4.1. Single-Wall Carbon Nanotubes

In 1997, Bockrath et al. [85] reported the first single-electron transport of a single bundle containing 60 single-wall carbon nanotubes (10,10) with a diameter of 1.4 nm at a temperature of 1.4 K. The device structure (Fig. 10, left inset) consists of a single nanotube rope and lithographically defined Au electrodes. The device has four contacts and allows different segments of the nanotube to be measured. The device was mounted on a standard chip carrier and contacts were wire bonded. A dc bias (V_g) was applied to the chip carrier base to which the sample was attached. This dc bias can be used as gate voltage V_g to modify the charge density along the tube. Figure 10 shows the I–V characteristics of the nanotube section between contacts 2 and 3 as a function of temperature T. The conductance is strongly suppressed near $V = 0$ for $T < 10$ K. Figure 11A shows conductance G versus gate voltage V_g at $T = 1.3$ K. The conductance curve consists of a series of sharp peaks separated by regions of very low conductance. The peak spacing varies significantly. The height of peaks also varies widely with the maximum peak reaching e^2/h, where h is the Planck constant. The peak amplitude decreases with T (Fig. 11B) while the peak width increases with T (Fig. 11C). These phenomena can be understood based on Coulomb blockade effect described in Section 2.3. In this device, transport occurs by tunneling through the isolated segment of the rope. Tunneling on or off this segment is governed by the single-electron addition. The period of the peaks in gate voltage, ΔV_g, is determined by the energy for adding an additional electron to the rope segment.

In the same year (1997), Tans and co-workers [86] at Delft University of Technology built molecular devices using a metallic (armchair) SWNT as a quantum wire. Figure 12 shows the structure of the device. An individual SWNT with a diameter of ~1 nm is lying across two Pt electrodes with a separation of 140 nm. The third electrode located ~450 nm
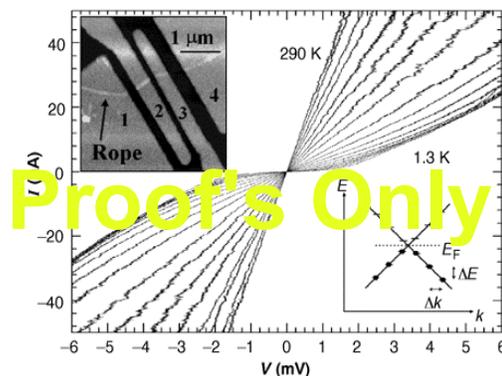

Figure 10. The I–V characteristics at a series of different temperatures for the rope segments between contacts 2 and 3. Left inset: AFM image of the fabricated device where the bright regions are metallic contacts. Right inset: Schematic energy-level diagram of the two 1D subbands near one of the two Dirac points with the quantized energy levels indicated. Reprinted with permission from [85], M. Bockrath et al., *Science* 275, 1922 (1997). © 1997, American Association for the Advancement of Science.
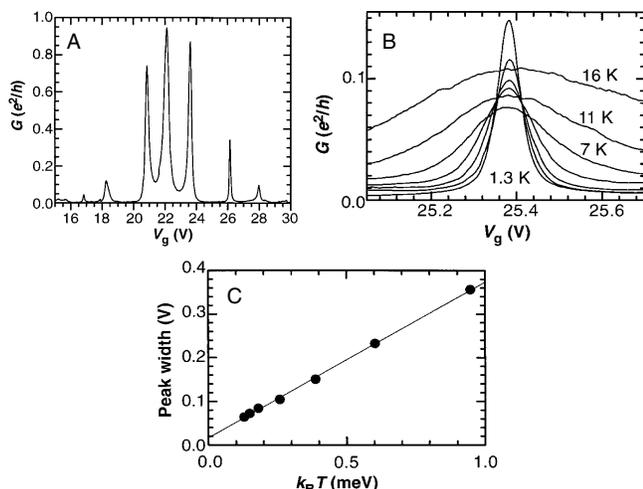
Figure 11. (A) Conductance G versus gate voltage V_g at $T = 1.3$ K for the rope segments 2 and 3. (B) Temperature dependence of a peak. (C) Width of the peak in (B) as a function of T. Reprinted with permission from [85], M. Bockrath et al., *Science* 275, 1922 (1997). © 1997, American Association for the Advancement of Science.

Figure 13. (a) Current–voltage curves of the nanotube at a gate voltage of 88.2 mV (trace A), 104.1 mV (trace B), and 120 mV (trace C). Inset: more I–V_{bias} curves with V_{gate} ranging from 50 mV (bottom curve) to 136 mV (top curve). (b) Current versus gate voltages at $V_{bias} = 30$ μV. Reprinted with permission from [86], S. J. Tans et al., *Nature* 386, 474 (1997). © 1997, Macmillan Publishers Ltd.

away from the nanotube functions as a gate. Their original idea is to build a single-electron transistor using a SWNT as a quantum wire. The electrical measurement was carried out at a low temperature of 5 mK. The typical current–voltage characteristics at various gate voltages are shown in Figure 13a. The coulomb charging effect is clearly observed. Coulomb charging occurs when the charging energy $E_c = (e^2/2C) \gg kT$. At low temperature, the Coulomb blockade effect can be observed. The two traces in Figure 13b were taken under identical conditions and show an occasional doubling of certain peaks. This bistability was regarded as the result of switching offset charges that shift the potential of the tube [86].

Chemical doping was used to achieve quantum dots and junctions for single-electron transistors [114]. Electrical measurements of the potassium (K) doped nanotube reveal single-electron charging at temperature up to 160 K [114]. The quantum dot is formed by inhomogeneous doping along the nanotube length [115–119]. The p–n–p junction

Figure 12. AFM tapping-mode image of a single-wall carbon nanotube on top of a Si/SiO$_2$ substrate with two 15-nm-thick Pt electrodes. Reprinted with permission from [86], S. J. Tans et al., *Nature* 386, 474 (1997). © 1997, Macmillan Publishers Ltd.
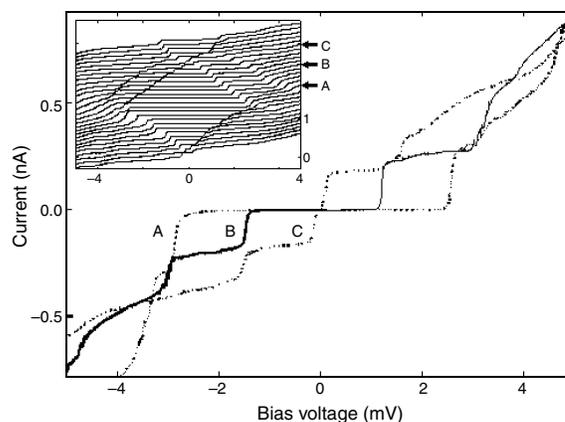
was obtained by chemical doping. The transport measurements of the junction showed that a well defined and highly reproducible on-tube single-electron transistor has been achieved [115]. It has been found that strong bends ("buckles") within metallic carbon nanotubes [2] act as nanometer-sized tunnel barriers for electron transport [116]. Single-electron transistors operating at room temperature have been fabricated by inducing two buckles in series within an individual metallic SWNT by manipulation with an AFM [117, 118]. The island with a length of 25 nm has been achieved and the resulting SET clearly showed the Coulomb blockade effect at room temperature [118]. Room temperature SETs have also been fabricated from SWNTs using V$_2$O$_5$ nanowires as masks for selective chemical doping [118]. Single-electron devices based on SWNTs with the line-shaped top gates [120], triple-barrier quantum dots [121], suspended quantum dots [122], field-induced p-type quantum dots [123], and kink-induced quantum dots [124] were fabricated. The microwave response of coupled quantum dots in SWNTs has also been measured [125]. The Coulomb oscillations for different microwave power were similar to those for different bias voltages without microwave.

Collins and co-workers [126] investigated electrical transport by sliding the STM tip along a nanotube. Figure 14 shows the schematic procedure for measuring nanotube characteristics using a single STM tip. From a position of stable tunneling (Fig. 14A), the STM tip was initially driven forward ~100 nm into the nanotube film (Fig. 14B). After retraction of the tip well beyond the normal tunneling range, nanotube material remained in electrical contact with the tip (Fig. 14C). Conductivity measurements were carried out by sliding the STM tip down along the nanotube while the tip remained electrically connected with the nanotube (Fig. 14D). The continuous motion of the tip allowed electrical characterization of different lengths of the nanotube. This technique results in a position-dependent electrical transport measurement along the extended lengths of selected nanotubes. A series of I–V curves were recorded
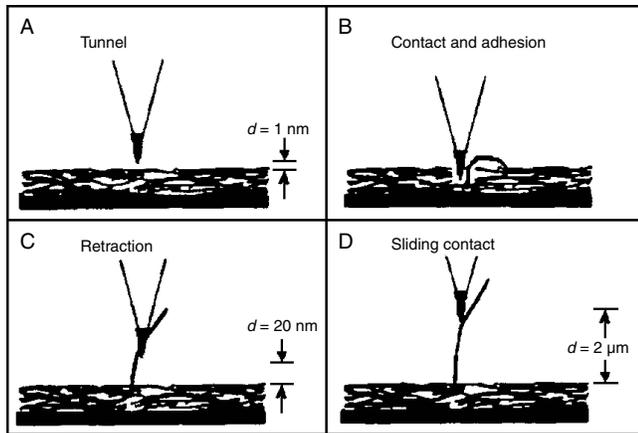
Figure 14. Schematic of the procedure for measuring nanotube characteristics with a single STM tip. Reprinted with permission from [126], P. G. Collins et al., *Science* 278, 100 (1997). © 1997, American Association for the Advancement of Science.

at positions 1600, 1850, 1950, and 2000 nm as shown in Figure 15. The first three curves are nonlinear but nearly symmetric. At a position of 2000 nm the *I–V* characteristics abruptly changed to a marked rectifying behavior (Fig. 15D). This response (Fig. 15D) was reproducible and persistent for positions up to 2300 nm before the nanotube was broken. It was suggested by Collins et al. [126] that the position-dependent behavior gives strong evidence for the existence of localized, well-defined, on-tube "nanodevices"
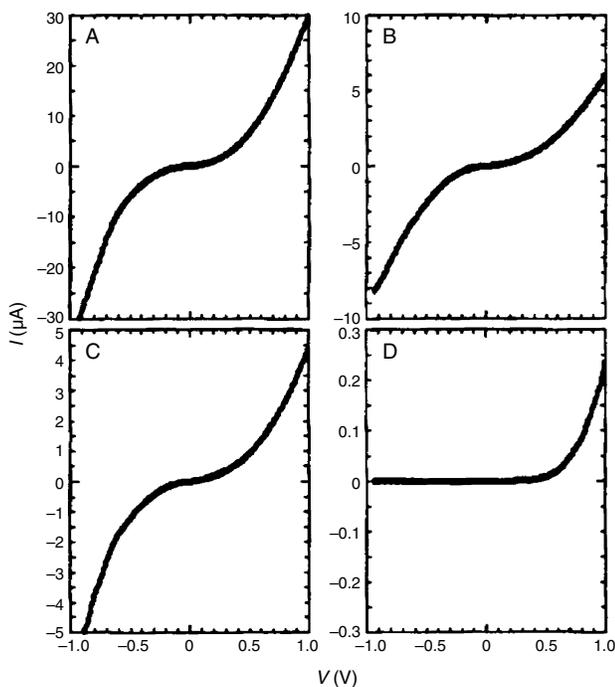
with response characteristics consistent with the theoretical predictions. The extreme changes in conductivity were caused by contact with the localized nanotube defects that greatly altered the local $N(E)$. Although the injected current predominantly indicates a graphitic behavior for the nanotube rope, a nanotube defect at the contact point would obscure and dominate the transport characteristics. For example, the existence of a pentagon–heptagon defect in the otherwise perfectly hexagonal nanotube wall fabric can lead to sharp discontinuities in the electronic density state along the tube axis. It is possible to have one portion of the nanotube with metallic characteristics almost seamlessly joined to another portion that is semiconducting. This "junction" constitutes a pure-carbon Schottky barrier. The sliding STM probe indicates exactly this type of behavior as its position moves along the length of a nanotube by only a few nanometers, indicating the existence of a localized nanotube nanodevice.

4.2. Multiwall Carbon Nanotubes

Although single-electron transistors were made first from SWNTs [85, 86], a few reports [127–132] can be found for fabrication of SETs using MWNTs. Roschier et al. [127] of Helsinki University fabricated single-electron transistors using MWNTs through manipulation by a SPM. Figure 16 shows the experimental procedure for rotating and moving a nanotube, and eventually the tube was set across the electrodes with a gap of ∼300 nm. The electrical measurements of the device were done at low temperatures
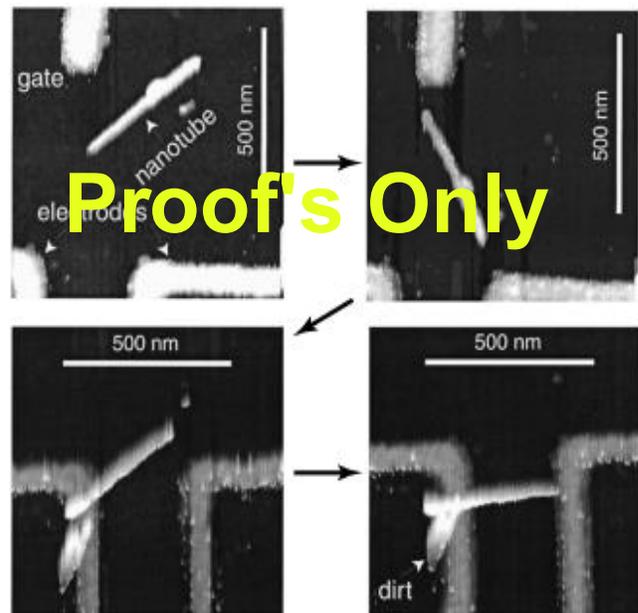

Figure 15. Different types of current–voltage characteristics, obtained for contact points at different heights of (A) 1600, (B) 1850, (C) 1950, and (D) 2000 nm along the carbon nanotube. Reprinted with permission from [126], P. G. Collins et al., *Science* 278, 100 (1997). © 1997, American Association for the Advancement of Science.

Figure 16. AFM images during moving process. The 410 nm long MWNT, the side gate, and the electrode structure are marked in the first frame. The last frame represents the measured configuration, where one end of the MWNT is well over the left electrode and the other end is lightly touching the right electrode. Reprinted with permission [128], L. Roschier et al., *Appl. Phys. Lett.* 75, 728 (1999). © 1999, American Institute of Physics.

down to 4 K. The measured I–V curves display a 15 mV wide zero current plateau across zero-voltage bias as shown in Figure 17. The Coulomb blockade effect is clearly observed below a few Kelvin and the nanotube behaves as a SET. The asymmetry of the gate modulation, illustrated in the inset for $V_{\text{bias}} = 10$ mV, indicates a substantial difference in the resistance of the tunnel junctions. There is a clear hysteresis in the I–V_{bias} curve at $T = 120$ mK. It is suggested that this phenomenon can be attributed to charge trapping, in which single electrons tunnel hysteretically across the concentric tubes. Roshier et al. [128] later constructed low-noise radio-frequency (rf) single-electron transistors using MWNTs. Contact resistance between a metal and a nanotube is commonly on the order of quantum resistance $R_Q = h/e^2 = 26.6$ kΩ. Hence, quantum fluctuations do not destroy charge quantization and thus it is possible to construct sensitive electrometers based on electrostatically controlled single-electron tunneling. The rf-SETs are the best electrometers at present [133]. As reported by Schoelkopf et al. [133] of Yale University, the sensitivity of rf-SETs based on Al islands approaches $1.2 \times 10^{-5} e/\sqrt{\text{Hz}}$, near the quantum limit at high frequencies. However, at frequencies below 1 kHz, these devices are plagued by the presence of $1/f^{\alpha}$ noise ($\alpha \sim$ 1–2). The origin of $1/f^{\alpha}$ noise is the trapping and detrapping of charges either in the vicinity of the island or on the surface of the nanotube or in the tunnel barrier [134, 135]. One way to reduce the $1/f^{\alpha}$ noise in SETs is to avoid contact of the central island with any dielectric material. In research by Roshier and co-workers [128], a freestanding MWNT across two electrodes was used as the island. The MWNT was moved onto the top of the electrodes by an AFM tip. The $1/f^{\alpha}$ noise of the SET is $6 \times 10^{-6} e/\sqrt{\text{Hz}}$ at 45 Hz, close to the performance in the best metallic SETs.
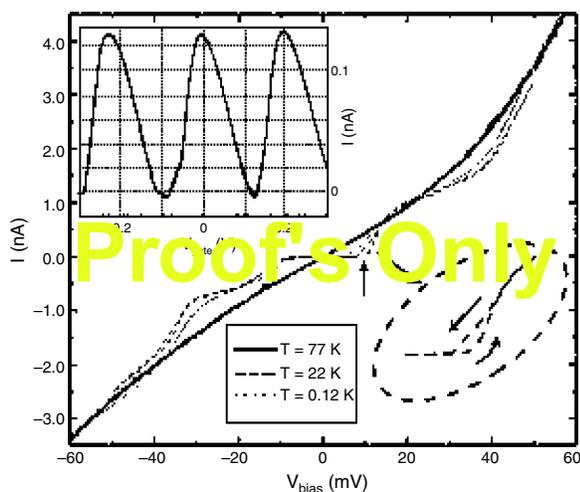

Figure 17. Measured I–V_{bias} curves at different temperatures when the gate is at zero bias. The inset shows the gate modulation at $V_{\text{bias}} = 10$ mV (indicated by the arrow) at $T = 120$ mK. The enlargement in the lower right corner shows the hysteretic behavior of the current. Reprinted with permission from [128], L. Roschier et al., *Appl. Phys. Lett.* 75, 728 (1999). © 1999, American Institute of Physics.

5. FIELD-EFFECT TRANSISTORS, LOGIC GATES, AND MEMORY DEVICES

5.1. Field-Effect Transistors

The significance of the paper by Tans et al. [86] is not in the quantum effect, but in the gate-induced modulation of conductance of the metallic nanotube. Field-effect transistors were first demonstrated using a single semiconducting SWNT by Tans et al. [136], and using both a SWNT and a MWNT by Avouris et al. [137–140]. Figure 18 shows the structure of the carbon nanotube field-effect transistor (CNTFET) [137]. The two electrodes are separated by 300 nm and gate oxide (SiO$_2$) is 140 nm. Figure 19 shows output characteristics of a SWNT-FET consisting of a single SWNT with a diameter of 1.6 nm for several values of the gate voltage. It is clearly seen that the source–drain current is modulated by electric field. The field effect of the MWNT-FET device was not observed [137]. The hole mobility is estimated to be 20 cm^2/V s. In 1999, Dai and co-workers [141] reported fabrication of FET using SWNTs controllably grown on substrates. Figure 20 shows the I–V curves at various gate voltages [141]. The asymmetry of the I–V curves was regarded as being inherent to the metal–tube–metal system. I–V curves after exchanging the source and drain show nearly unchanged asymmetry. These results suggest that the observed asymmetry is not caused by asymmetrical parameters such as different contact resistance at the two metal–tube contacts [141]. It was suggested that the asymmetry of I–V curves is due to high source–drain bias [141]. The transconductance was estimated to be 0.1 mS/μm.

5.1.1. Scaling of CNTFET

Theoretical studies [142] showed that the performance can be significantly improved if the channel length and gate oxide can be further scaled down. The I–V characteristics are similar to the ballistic Si MOSFETs except for the occurrence of quantized channel conductance. Because of ballistic transport, the average carrier velocity reaches 2.7×10^7 cm/s [145]. Theoretical studies [143] also show that the CNTFET can be scaled down to at least 5 nm. Because of the ballistic transport, there is no energy dissipation except at contacts, and terahertz operation may be possible. Recently Wind and co-workers at IBM [144] improved their CNTFET
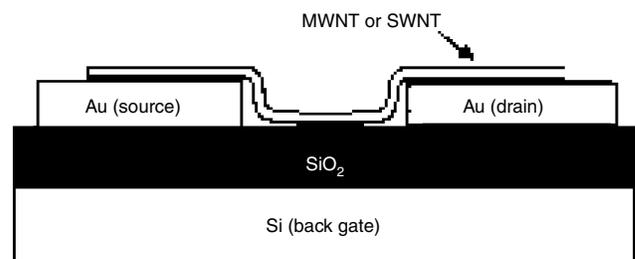

Figure 18. Schematic cross-section of the FET devices. A single nanotube of either multiwall or single-wall type bridges the gap between two gold electrodes. The silicon substrate is used as back gate. Reprinted with permission from [137], R. Martel et al., *Appl. Phys. Lett.* 73, 2447 (1998). © 1998, American Institute of Physics.
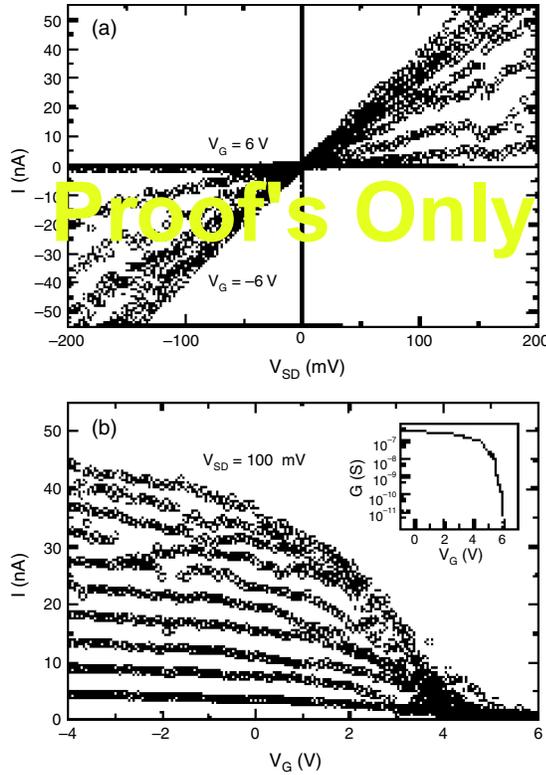
Figure 19. Output and transfer characteristics of a SWNT-FET: (a) I–V_{SD} curves measured for $V_G = -6$, 0, 1, 2, 3, 4, 5, and 6 V. (b) I–V_G curves for $V_{SD} = 10$–100 mV in steps of 10 mV. The inset shows that the gate modulates the conductance by 5 orders of magnitude ($V_{SD} = 10$ mV). Reprinted with permission from [137], R. Martel et al., *Appl. Phys. Lett.* 73, 2447 (1998). © 1998, American Institute of Physics.

structure with top gate and very thin gate oxide (15 nm). Figure 21 shows the device structure and its output characteristics. A single-wall carbon nanotube with a diameter of 1.4 nm was used as a semiconductor nanowire. The source and drain were defined by e-beam lithography with a gate length of 260 nm. I–V curves show excellent saturation and on–off ratio of 10^5. Table 1 shows a comparison of key device performance parameters for a 260 nm gate length p-type CNTFET with those of state-of-the-art Si MOS transistors, a 15 nm gate Si p-type MOSFET [145] and a 50 nm gate SOI p-type MOSFET [146]. It can be found that a CNTFET has superior performance over Si MOSFETs. A CNTFET exhibits a much higher ON current ($I_{on} = 2100$ μA/μm), reasonable OFF current ($I_{off} = 150$ nA/μm), and very high transconductance (2321 μS/μm). It should be noted that the transconductance of the 15 nm gate Si p-MOSFET is only 975 μS/μm [145].

5.1.2. High Mobility

In [144], Wind et al. did not characterize the hole mobility during transport. I will analyze the hole mobility as follows. Because the I–V curves follow the classical transport model, the transconductance in saturation is expressed as [147]

$$G_{msat} = \frac{\mu_p C_{ox} W}{2L} |V_G - V_T|$$

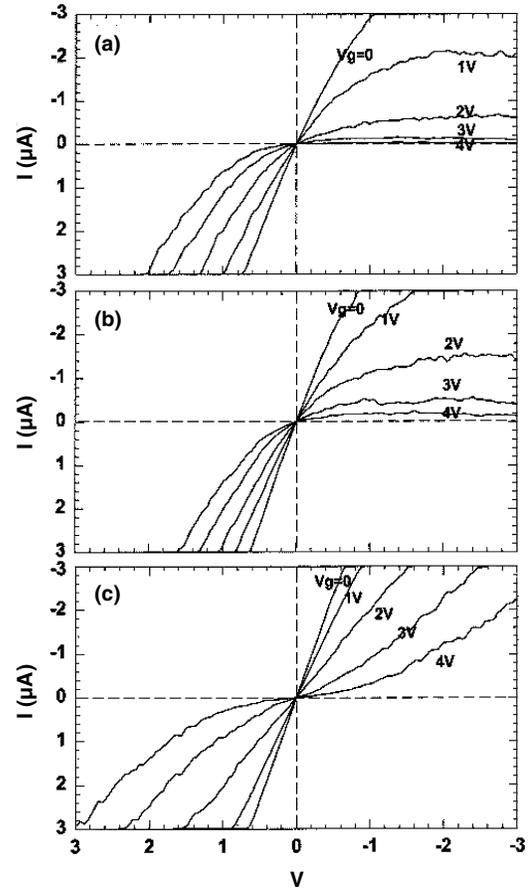**Figure 20.** (a) Room-temperature I–V curves recorded with sample S1 for V in the range 3 to -3 V under various gate voltages. (b) I–V curves recorded after exchanging the source–drain electrodes. (c) Symmetrical I–V curves obtained by scanning V while biasing the two electrodes at $-V/2$ and $V/2$, respectively. Reprinted with permission from [141], H. Dai et al., *J. Phys. Chem. B* 103, 11246 (1999). © 1999, American Chemical Society.

where μ_p is the hole mobility. L and W are the gate length and gate width separately. C_{ox} is the gate oxide capacitance. V_G is the gate voltage and V_T is threshold voltage (-0.5 V). The gate width is considered to be half of the perimeter of the CNT (diameter = 1.4 nm). Thus the mobility can be calculated using

$$\mu_p = \frac{G_{msat} 2L}{C_{ox} W |V_G - V_T|}$$

Based on the given data of the transistor structure, the hole mobility is 2018 cm^2 V^{-1} s^{-1}. This is much larger than the ideal hole mobility in bulk Si ($\sim$400 cm^2 V^{-1} s^{-1}) and 200$\times$ higher than the hole mobility (12 cm^2 V^{-1} s^{-1}) derived from the 15 nm gate p-Si MOSFET [145]. *These surprising data indicate the potential of carbon nanotubes for high-speed device application similar to III–V compound semiconductors such as GaAs.* It was reported that SWNTs are extremely pure systems with large Fermi velocities of $v_F = 10^6$ m/s and ballistic transport over long distance [65, 91, 148]. Considering its unique 1D quantum wire electronic band structure and ballistic transport over long distance, it is highly possible for SWNTs to have extremely high mobility.
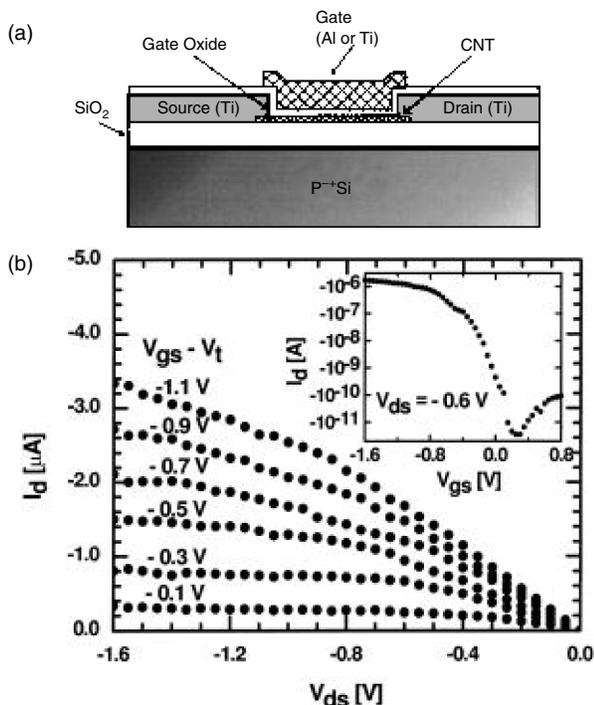
Figure 21. Schematic cross-section of top gate CNFET showing the gate and source and drain electrodes. (b) Output characteristic of a top gate p-type CNFET with a Ti gate and a gate oxide thickness of 15 nm. The gate voltage values range from -0.1 to -1.1 V above the threshold voltage, which is -0.5 V. Inset: Transfer characteristic of the CNFET for $V_{ds} = -0.6$ V. Reprinted with permission from [144], S. J. Wind et al., *Appl. Phys. Lett.* 80, 3817 (2002). © 2002, American Institute of Physics.

The high mobility of nanotube transistors estimated by the present author has been confirmed by Rosenblat et al. [149] and Kruger et al. [150]. Rosenblat et al. [149] constructed a carbon nanotube transistor using an electrolyte as gate, which was inspired by the study of doping effects using electrochemical gating [150, 151]. Figure 22 shows the device structure [149]. Catalyst islands containing $Fe(NO_3)_3 \cdot 9H_2O$, $MoO_2(acac)_2$, and alumina nanoparticles were defined on SiO_2. Carbon nanotubes were then grown by chemical vapor deposition. The source and drain with a separation of 1–3 μm (channel length) were defined using

Table 1. Comparison of key device performance parameters for a 260 nm gate length p-type CNTFET with those of state-of-the-art Si MOS transistors: a 15 nm-gate p-type Si MOSFET and a 50 nm gate p-type SOI MOSFET.

Types of transistors	CNTFET [144]	Si MOSFET [145]	SOI MOSFET [146]
Gate length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
Threshold voltage (V)	-0.5	-0.1	-0.2
I_{ON} (μA/μm) @ $V_{DS} = V_{GS} - V_T = 1$ V	2100	265	650
I_{OFF} (nA/μm)	150	$\sim$500	9
Subthreshold slope (mV/dec)	130	$\sim$100	70
Transconductance (μS/μm)	2321	975	650

Source: Adapted with permission from [144], S. J. Wind et al., *Appl. Phys. Lett.* 80, 3817 (2002). © 2002, American Institute of Physics.
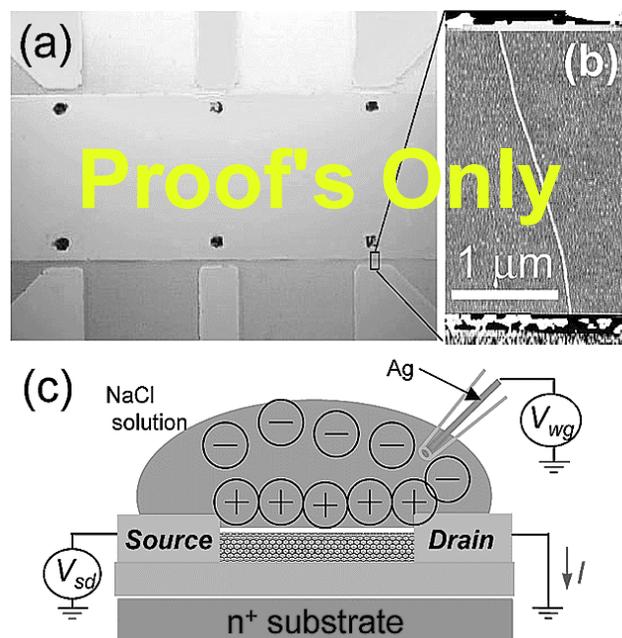

Figure 22. Optical micrograph of the device. Six catalyst pads (dark) can be seen inside the area of the common electrode. Correspondingly, there are six source electrodes for electrical connection to tubes. (b) AFM image of a tube between two electrodes. The tube diameter is 1.9 nm. (c) Schematic of the electrolyte gate measurement. A water gate voltage V_{wg} is applied to droplets through a silver wire. Reprinted with permission from [149], S. Rosenblat et al., *Nano Lett.* 2, 869 (2002). © 2002, American Chemical Society.

photolithography and a lift-off process. A micropipet is used to place a small ($\sim$10–20 μm) saltwater droplet (NaCl solution) over the nanotube device. A voltage V_{wg} applied to a silver wire in the pipet is used to establish the electrochemical potential in the electrolyte relative to the device. Then the electrolyte functions as a liquid gate. The output characteristics of the electrolyte carbon nanotube FET are similar to those in Figure 21. The transconductance of the transistor reaches its maximum $\sim$20 μS at a gate voltage of -0.8 V. The mobility inferred from the conductance measurement is in the range of 1000 to 4000 cm^2 V^{-1} s^{-1}. The maximum on-state conductance is also shown for the same samples. Values on the order of e^2/h are routinely obtained, within a factor of 4 of the theoretical limit of $4e^2/h$. Fuhrer et al. [152] reported the hole mobility in a SWNT of 9000 cm^2 V^{-1} s^{-1}, which is the highest value ever reported.

In addition, the field effect is clearly shown even at a temperature of 5 K with a spikelike conductance, which is attributed to the van Hove singularities [153]. AFM tips were used to apply pointlike local gates to manipulate the electrical properties of an individual SWNT contacted by Ti electrodes [154]. The AFM tip contacting on a semiconducting SWNT causes depletion at a local point, leading to orders of magnitude decrease of the nanotube conductance, while local gating to a metallic SWNT leads to no change in conductance [154]. Theoretical study also suggests that a quantum dot is formed because of the induced n-type together with the p-type near the metal contacts when a positive gate voltage is applied on the p-type SWNT [155]. The induced quantum dot enhances the conductance.

Because the energy bandgaps of semiconducting SWNTs are inversely proportional to their diameter, large-diameter SWNTs have smaller energy bandgaps. Transistors made of large-diameter SWNTs exhibit ambipolar field-effect transistor behavior [156, 157]. Theoretical study showed that the energy gap of a semiconducting nanotube can be narrowed, when the tube is placed in an electric field perpendicular to the tube axis (e.g., in the FET case) [158]. This band-structure modulation may affect the electrical properties of CNTFETs. No experimental research has been reported regarding this phenomenon. For characterization of the semiconductor/oxide interface, capacitance–voltage measurement is usually carried out on MOS capacitors. Theoretical study showed that the calculated C–V curves reflect the local peaks of the 1D DOS in the nanotube [159]. This might be used for diagnose the electronic structure of nanotubes, providing a more convenient approach than STM. However, experimental measurement of the capacitance in nanoscale is not easy because the accumulation capacitance of a 1-μm long nanotube MOS capacitor is only 1.5×10^{-4} pf or 1.5 pf/cm [159].

5.2. Logic Gates

In 2001, several groups [160–162] demonstrated logic circuits using carbon nanotube transistors. Bachtold et al. [160] showed inverter, NOR gate, static random access memory (SRAM), and ring oscillator. Derycke et al. [161] and Liu et al. [162] showed the CMOS inverter using both n- and p-channel CNTFETs. Figure 23 shows individual device structure and layout [160]. Unlike the previous nanotube transistor structure using back gate, which applies the same gate voltage to all transistors, the transistor structure consists of a microfabricated Al wire with native Al_2O_3 as gate insulator, which lies beneath a semiconducting nanotube that is electrically contacted to two Au electrodes. The channel length is about 100 nm and gate oxide thickness is about a few nanometers. This layout allows the integration of multiple nanotube FETs. The transistor is a p-type enhancement mode FET with transconductance of 0.3 μS and on–off ratio of at least 10^5. The transistor can operate at an ON current of 100 nA and an OFF current of 1 pA. The basic logic elements such as inverter, NOR gate, SRAM, and ring oscillator were constructed as shown in Figure 24. The inverter exhibits very good transfer characteristics. When input voltage is −1.5 V (logic 1), the output voltage is 0 V (logic 0). When the input voltage is switched to 0 (logic 0), the output becomes −1.5 (logic 1). Although the transition is not as sharp as a Si MOSFET, it is still competitive. Because this inverter is constructed using a single transistor, the standby current is still high. The ring oscillator shows good oscillation waveforms although the oscillation frequency is low in this pioneer stage. The inverters have been constructed using complementary nanotube FETs similar to Si CMOS structure (complementary MOS), leading to minimum standby power consumption [161, 162]. Figure 25 shows the CMOS inverter based on both n- and p-CNTFETs and its transfer characteristic [161]. A single nanotube bundle is positioned over the gold electrodes to produce two p-type CNTFETs in series. The device is covered by PMMA and a window is opened by e-beam lithography to expose part of the nanotube. Potassium is then evaporated through
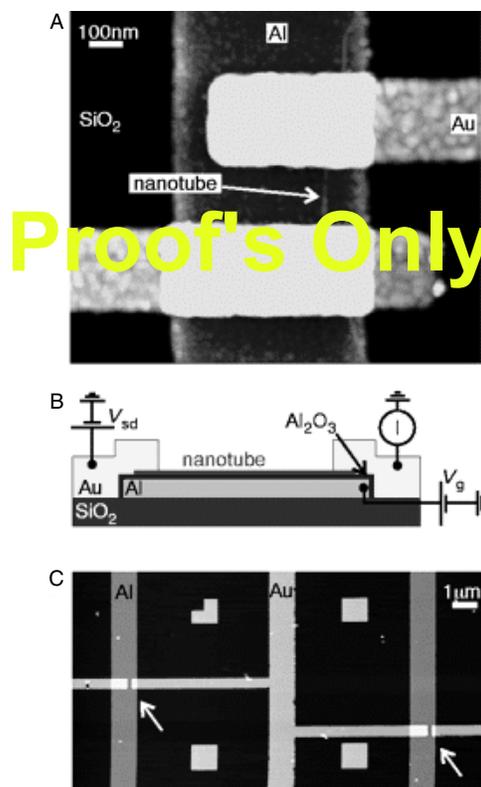

Figure 23. Device layout. (A) Height image of a single-nanotube transistor, acquired with an atomic force microscope. (B) Schematic side view of the device. (C) Height-mode atomic force microscope image of two nanotube transistors connected by a Au interconnect wire. The arrows indicate the position of the transistors. Reprinted with permission from [160], A. Bachtold et al., *Science* 294, 1317 (2001). © 2001, American Association for the Advancement of Science.

this window to produce an n-CNTFET, while the other CNTFET remains p-type. The transfer characteristics show much better transition region (more steep slope).

5.3. Memory Devices

A concept for molecular electronics exploiting carbon nanotubes as both molecular device elements and molecular wires for reading and writing information has been proposed [163]. Each device is based on suspended, crossed nanotube geometry that leads to bistable, electrostatically switchable ON/OFF states. The device elements are naturally addressable in large arrays by the carbon nanotube molecular wires making up the devices. These reversible, bistable device elements could be used to construct nonvolatile random access memory and logic function tables at an integration level approaching 10^{12} elements per cm^2, and an element operation frequency in excess of 100 GHz [163]. However, strictly speaking, these memory devices or logic gates are not made of CNTFETs. Several groups [152, 164–166] reported fabrication of memory devices using nanotube field-effect transistors. Air-stable n-type, ambipolar CNTFETs were fabricated and used in nanoscale memory cells [164]. The n-type transistors are achieved by annealing nanotubes in hydrogen gas and contacting them by cobalt electrodes. Due to their nanoscale capacitance, CNTFETs
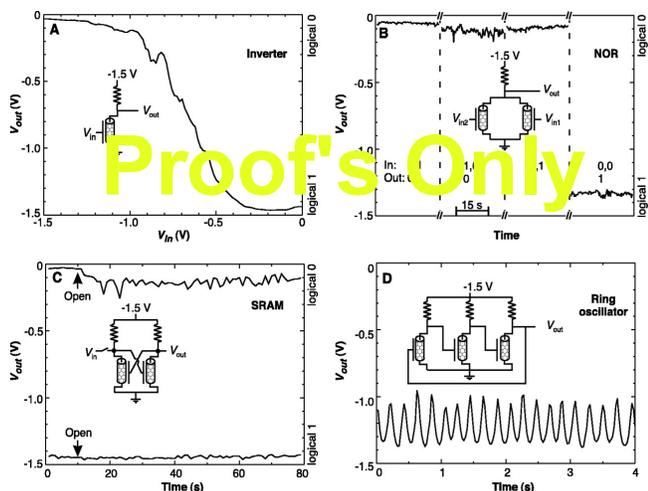
Figure 24. Demonstration of one-, two-, and three-transistor logic circuits with carbon nanotube FETs. (A) Output voltage as a function of the input voltage of a nanotube inverter. Inset: Schematic of the electronic circuit. The resistance is 100 MΩ. (B) Output voltage of a nanotube NOR for the four possible input states (1,1), (1,0), (0,1), and (0,0). The resistance is 50 MΩ. (C) Output voltage of a flip–flop memory cell (SRAM) composed of two nanotube FETs. The two resistances are 100 MΩ and 2 GΩ. (D) Output voltage as a function of time for a nanotube ring oscillator. The three resistances are 100 MΩ, 100 MΩ, and 2 GΩ. Reprinted with permission from [160], A. Bachtold et al., *Science* 294, 1317 (2001). © 2001, American Association for the Advancement of Science.

are extremely sensitive to the presence of individual charges around the channel, which can be used for data storage that operate at the few-electron level [165]. Figure 26 shows the threshold voltage shift due to storage of charges (a,b,c), device structure (d), and the voltage signal (V_{out}) due to charge storage [164]. In addition, the data-storage stability of over 12 days has been achieved [165].

6. DOPING, JUNCTIONS, AND METAL–NANOTUBE CONTACTS

A key technology advancement for the success of semiconductor industry is achievement of *n*- and *p*-type doping, junctions, and Ohmic contacts between metal and
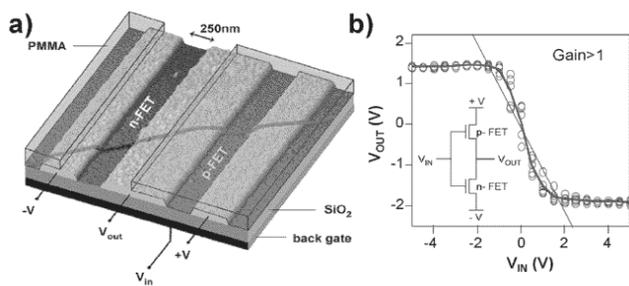

Figure 25. (a) AFM image showing an intramolecular logic gate. (b) Characteristics of the resulting intramolecular voltage inverter. The thin straight line corresponds to an output/input gain of one. Reprinted with permission from [161], V. Derycke et al., *Nano Lett.* 1, 453 (2001). © 2001, American Chemical Society.
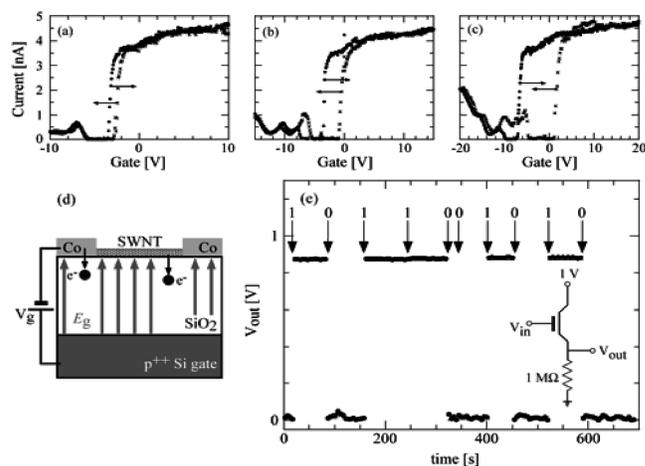

Figure 26. (a)–(c) High vacuum I–V_g data at $V_{ds} = 0.5$ mV. Device hysteresis increases steadily with increasing V_g due to avalanche charge injection into bulk oxide traps. (d) Diagram of avalanche injection of electrons into bulk oxide traps from the CNFET channel. (e) Data from CNFET-based nonvolatile molecular memory cell. A series of bits is written into the cell (see text) and the cell contents are continuously monitored as a voltage signal (V_{out}) in the circuit shown in the inset. Reprinted with permission from [164], M. Radosavljevic et al., *Nano Lett.* 2, 761 (2002). © 2002, American Chemical Society.

semiconductor. It is critical to achieve doping, *pn* junctions, and Ohmic contacts for carbon nanotubes so that nanotube electronics may evolve into a large industry.

6.1. Chemical Doping

Antonov and Johnson [167] observed current rectification in a molecular diode consisting of a semiconducting SWNT and an impurity. It was suggested that rectification resulted from the local effect of the impurity on the tube's band structure. It is not clear what type of impurity it was. Lee et al. [168] reported doping of SWNTs by vapor-phase reactions with bromine and potassium. Doping decreases the resistivity of SWNTs at 300 K by up to a factor of 30 and enlarges the region where the temperature coefficient of resistance is positive, which is the signature of metallic behavior. It was reported [169, 170] that potassium (K) doping of SWNTs creates *n*-type carrier (electrons). The doping effects were studied using the transistor structure. The SWNT ropes were placed on top of Au electrodes that have 500 nm separation. The electrodes were fabricated on the oxidized n^+-Si substrate which serves as gate. The Au electrodes serve as source and drain. Figure 27 shows conductance vs gate voltage for an undoped nanotube rope (open circles) and an nanotube doped with potassium (solid circle) [169]. For the undoped nanotube, the conductance increases with decreasing gate voltage, indicating *p*-type behavior. For the K-doped nanotube, the conductance increases with increasing gate voltage, indicating *n*-type behavior. The typical values for the carrier density are found to be $\sim$100–1000 electrons/μm and the effective mobility of electrons is $\mu_{eff} \sim$ 20–60 in early time [169]. Derycke et al. [171] reported two methods for conversion of SWNTs from *p*-type to *n*-type. The first method involves conventional doping with an electron donor and the second
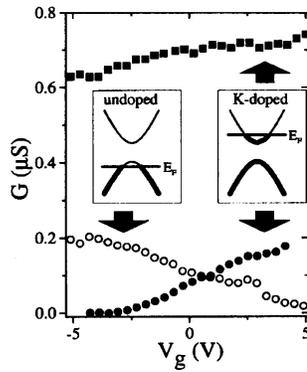
Figure 27. The conductance decreases with increasing gate voltage for an undoped sample (open circles), indicating *p*-type behavior. Left inset shows the energy band corresponding to this case. The conductance increases with increasing gate voltage after potassium doping at a high doping level (solid squares) and at a low doping level (solid circles). Right inset shows the energy band corresponding to this situation. Reprinted with permission from [169], M. Bockrath et al., *Phys. Rev. B* 61, R10606 (2000). © 2000, American Physical Society.

consists of annealing the metal nanotube contacts in vacuum to remove adsorbed oxygen. It has been found that the main effect of oxygen adsorption is not to dope the bulk of the nanotube, but to modify the Schottky barriers at the metal–semiconductor contacts [172, 173]. It also found that boron-doped MWNTs showed an enhanced room temperature conductivity [174]. However, theoretical calculation showed that H_2O adsorption on a SWNT reduces conductance [175].

6.2. Junctions and Metal–Nanotube Contacts

Zhou et al. [176] published the first attempt for controllable chemical doping of individual carbon nanotubes to achieve *pn* junctions. Figure 28 shows the device structure for potassium doping and the resulting energy band structure [176]. The SWNT used in the doping experiments has a diameter of ∼2 nm and a length of 3.5 μm and is placed across two metal electrodes. A back gate is used to modulate the carrier concentration by applying voltage on the gate. A polymethylmethacrylate (PMMA) layer of 340 nm thickness covers the left half of the nanotube, leaving the right half exposed. Prior to doping, SWNT is a *p*-type semiconductor. Potassium doping of the SWNT is carried out in vacuum by electrical heating of a potassium source. Figure 29A shows the I–V_g curves [176]. When $V_g < -1$ V (Regime I), hole accumulation is achieved in the SWNT, leading to p^+ in the PMMA protected area due to increase in hole concentration and n in the exposed region due to compensation of electrons. In Regime II, electron concentration begins to increase, resulting in p^+n^+ junction. I–V curves of p^+n and p^+n^+ junctions are shown in Figure 29B and C. In the forward bias regime, a nice *pn* junction diode is demonstrated. However, the reverse bias breakdown voltage is too small to be qualified as a diode [176]. Anyway, this is the first result showing some possibility for fabrication of nanotube-based *pn* junction diodes.
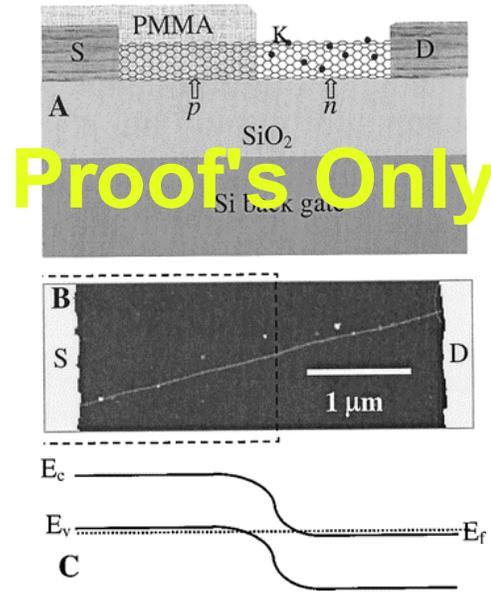

Figure 28. An SWNT with modulated chemical doping. (A) Device scheme with the SWNT contacted by two Ni/Au electrodes. The right half of the SWNT is doped by evaporating K atoms (black dots) from an alkaline metal at 10^{-6} Torr. (B) Atomic force microscopy image of the SWNT recorded before PMMA coating of the left half and doping. The bright regions at the two ends are the electrodes. Dashed lines are drawn to highlight the later PMMA-covered region. (C) A band diagram for the system. Reprinted with permission from [176], C. Zhou et al., *Science* 290, 1552 (2000). © 2000, American Association for the Advancement of Science.

Figure 29. Electrical properties of the modulation-doped SWNT at room temperature. (A) Current versus gate-voltage I–V_g curve recorded under a bias voltage $V = 1$ mV. The drawings show the band diagrams in four regimes. (B) and (C) I–V curves recorded in Regimes I and II. The star and triangle in (A) marks the gate voltages for the I–V curves in (B) and (C), respectively. Reprinted with permission from [176], C. Zhou et al., *Science* 290, 1552 (2000). © 2000, American Association for the Advancement of Science.
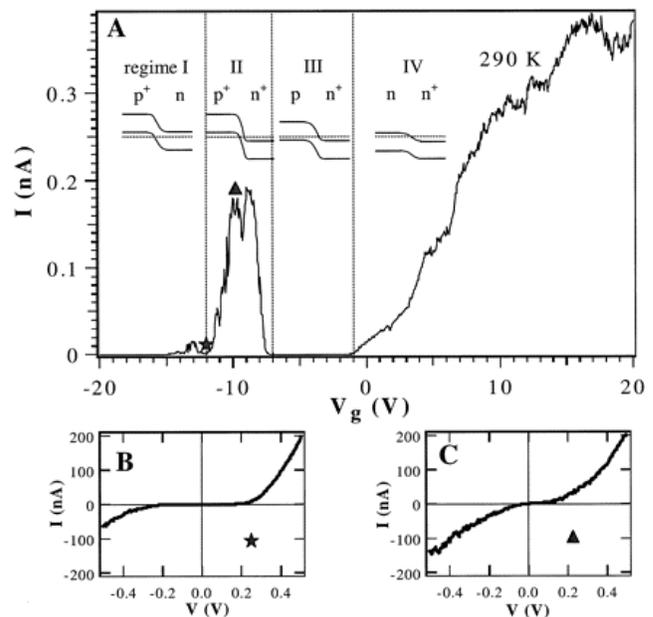
Based on theoretical calculation, Chico et al. [177] proposed metal/semiconductor or semiconductor/semiconductor junctions, made of SWNTs, and based on the introduction of topological defects in nanotubes. By introducing a pentagon and a heptagon into the hexagonal carbon lattice, two tube segments with different electronic structures can be seamlessly fused together to create semiconductor–semiconductor or metal–semiconductor junctions [172, 178, 179]. Two carbon nanotubes have also been fused together by high electric field [180]. The CN_x/nanotube junctions have been synthesized by a microwave plasma assisted CVD method [181]. It is of particular interest that two SWNTs were crossed over each other to form junctions [182]. Theoretical study also suggests that negative differential resistance may be observed in metal–nanotube–metal structures [183]. Figure 30 shows the AFM image of a nanotube junction with a sharp kink of about 40° [172]. The kink consists of five to seven defects. Figure 31 shows the I–V characteristics of the kink metal–semiconductor junction [172]. The rectification effect is clearly seen in the figure. A model has been proposed for the kink-shaped carbon nanotube Schottky diode, where the gate voltage modulation is included [184, 185]. It has been observed that the nanotube Schottky diodes [172, 179] and the nanotube pn junctions [176] exhibit much lower reverse-bias breakdown voltage than conventional, micrometer-size Schottky diodes and pn junctions. A theoretical model has been proposed to describe the potential barrier shape in ultrasmall Schottky diodes [186]. It is suggested that for diodes smaller than a characteristic length l_c (e.g., 80 nm for $N_d = 10^{17}$ cm^{-3}), Schottky barrier thickness becomes a function of the diode size. Consequently, the contribution of tunneling to the total conductance is dramatically enhanced, resulting in lower reverse breakdown voltage in nanoscale diodes [186]. The carbon nanotube "T" junction with heptagons or pentagons for joints has been proposed theoretically [187]. However, experimentally no "T" junction has been observed. Instead, "Y" junctions have been produced through an anodic aluminum oxide (AAO) template [188, 189] and directly on substrates [190–196]. Theoretical calculation confirms the rectification
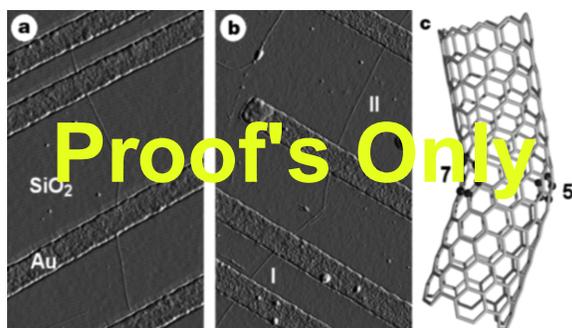

Figure 30. Tapping-mode atomic force microscope amplitude images of examples of nanotube junction devices. (a) and (b) Nanotubes that contain a single kink of 36° and 41° respectively. (c) Illustration of the carbon-bond network of a kink junction constructed between an "armchair" tube and a "zigzag" tube, where 5 denotes a pentagon, 7 denotes a heptagon, and the atoms in the pentagon and heptagon are highlighted by dark balls. Reprinted with permission from [172], Z. Yao et al., *Nature* 402, 273 (1999). © 1999, Macmillan Publishers Ltd.
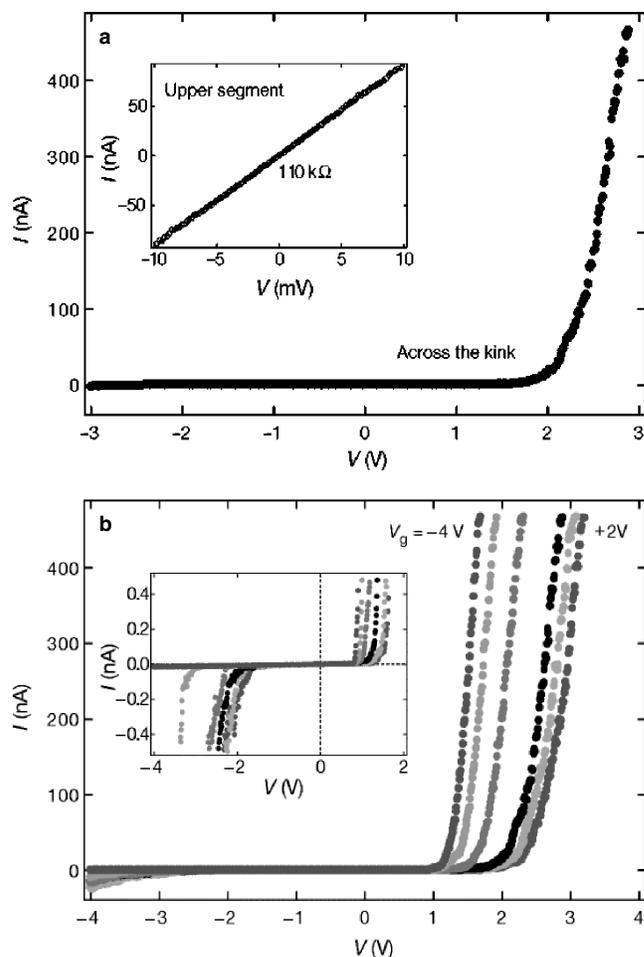

Figure 31. Current–voltage characteristics across the metal–semiconductor junction of (a), showing rectifying behavior. The data are taken at 100 K. The results at room temperature are similar, but the data are noisier. Inset in (a): the I–V curve for the upper straight segment measured at room temperature. In (a), the gate is grounded. In (b): the gate voltages from right to left are 2, 1, 0, −1, −2, and −4 V respectively. Inset in (b): expanded view of the small-current region which shows more clearly the onset of conduction for both bias polarities. Reprinted with permission from [172], Z. Yao et al., *Nature* 402, 273 (1999). © 1999, Macmillan Publishers Ltd.

effect of "Y" junctions [197–199]. When the positively biased metal–nanotube contact (source electrode) is locally gated with a negative gate voltage, a dramatic increase in transport current occurs because the Schottky barrier thickness is reduced due to accumulation of holes near the contact [200]. For the negatively biased metal–nanotube contacts, the gate voltage has no effect on transport because no Schottky barrier exists there [200]. Therefore, by positioning the gate locally near one of the contacts, the nanotube FET is converted into a rectifying diode [200].

Zhang et al. [201] fabricated the first real Ohmic contacts between SWNTs and Ti by solid solid reaction: C (nanotubes) + M (solid) → MC (solid), where M is metal. The reaction was performed at a temperature ranging from 800 to 1000 °C in ultrahigh vacuum or an inert atmosphere to avoid volatile reactant [201]. The continuous transformation of the SWNT to carbide is controlled by the diffusion of

M to the C/M interface. The I–V curves showed a straight line when the bias voltage is swept from -1 to 1 V, indicating a true *Ohmic contact* [201]. The resistance at the contact is ~ 0.3 kΩ [201], much better than the contact resistance (~ 20 kΩ) for the direct metal/nanotube contacts [202, 203].

7. NANOTUBE-BASED NANOFABRICATION

Carbon nanotubes exhibit Coulomb-blockade effects, ballistic transport, and field effects. Of particular importance is the field effect that may lead to the carbon nanotube electronics era. However, a critical issue for successful realization of carbon nanotube electronics is how to manipulate the nanotubes so that large-scale manufacturing is possible.

7.1. Manipulation of Nanotubes Using AFM and STM

Since discovery of carbon nanotubes [1], for electronic device research, the majority of research has been focused on manipulation of carbon nanotubes using the STM or AFM [86, 118, 127, 163, 203–223]. Tans et al. [86] deposited SWNTs on the SiO_2/Si substrate which had patterned metal electrodes. An individual nanotube wire was put across the Pt electrodes, which was imaged by an AFM. Physical manipulation of nanotubes with the AFM tip, like rolling, sliding, bending, and buckling, has been used to investigate mechanical properties of nanotubes [211, 212]. Roschier et al. [127] positioned a semiconducting multiwalled nanotube between two gold electrodes at the SiO_2 surface. The 410 nm long MWNT was manipulated and positioned on the gold electrodes by the AFM tip. Soh et al. [203] synthesized SWNTs on the patterned catalytic islands, which are contacted with metal pads. Lefebvre et al. [204] developed a method to assemble SWNT circuits using a tapping mode AFM. Nanotubes can be controllably translated, rotated, cut, and placed on top of one another by varying the tip–sample force and the tip speed. These operations can construct complex nanotube circuits. Of particular interest is that the suspended SWNT can be deformed locally by the AFM tip, leading to a decrease in conductance of the nanotube by two orders of magnitude [217–219]. This effect can be used to construct nanoelectromechanical devices. Tight-binding simulation showed that this effect is caused by the formation sp^3 bonds because of the mechanical pushing action of the tip [217, 218]. Collins et al. at IBM [205] demonstrated a simple method for permanently modifying MWNTs by using current-induced breakdown to eliminate individual shells one at a time. Carbon nanotubes can withstand remarkable current densities, exceeding 10^9 A/cm^2, because of their strong carbon–carbon bonding. However, at high enough current nanotubes ultimately fail. In MWNTs, this failure occurs in air at a certain threshold power through the rapid oxidation of the outermost carbon shell. The mechanism for the breakdown initiation is the current-induced defect formation. By using the electrical breakdown technique, they can remove the MWNT shells one by one. This controlled breakdown technique is also performed with the help of STM or AFM. Study of the reliability and current carrying capacity showed that under high current density ($>10^9$ A/cm^2) no observable failure in the nanotube structure and no measureable change in the resistance are detected at temperatures up to 250 °C and for time scales up to 2 weeks [224]. *Although these processes and techniques are especially useful for study of nanotubes' physical properties, they may not be appropriate for large-scale fabrication of nanotube-based devices and circuits with high yield.*

7.2. Controllable Growth and Placement of Nanotubes

Before we can think about building sophisticated nanotube-based circuitry, we must find how to grow the nanotubes in specific locations, orientations, shapes, and sizes, as well as how to construct nanotube devices at specific locations and how to connect nanotube devices with each other.

7.2.1. Vertically Aligned Carbon Nanotubes

Li et al. [225, 226] reported the first large-scale synthesis of vertically aligned carbon nanotubes by using CVD catalyzed by iron nanoparticles embedded in mesoporous silca. Vertically aligned arrays of isolated tubes with spacing between the tubes of about 100 nm were controllable through the pores. This method has been extended to grow freestanding carbon nanotubes on glass substrates at lower temperature (<700 °C) using nickel film as catalysts by CVD [227–229] and also on Si substrates [231]. Because the mesoporous structure of silica was not uniform, the controllability of tubes was not very good. It is well known that the porous structure of AAO film exhibits hexagonal close-packed nanopores with large-scale periodicity and high densities [232–234]. Highly ordered and vertically aligned carbon nanotube arrays was obtained when growth of nanotubes was carried out on AAO porous structure with cobalt particles deposited into the bottom of the pores [235–241]. Figure 32 shows the procedure for fabrication and growth and the scanning electron microscope (SEM) image of arrays of nanotubes [236]. It should be noted that these highly ordered CNT arrays were successfully fabricated on aluminum substrates. In order to incorporate the carbon nanotubes into the Si electronics, growth of aligned nanotubes on Si substrates is imperative. AAO films were cracked at about 300–400 °C, whereas AAO on N_b was not damaged at 1100 °C in He gas because the thermal expansion coefficient of N_b is close to that of AAO. It is suggested that the N_b layer under AAO may afford the durability for the high temperature process [242]. CNTs were grown on the AAO film based on 100-nm N_b film [242]. Unfortunately, the as-grown nanotubes were not uniformly controllable and sparse nanotubes were grown [242]. Hu et al. at the University of Kentucky [243, 244] successfully fabricated highly ordered CNT arrays on *silicon substrate* using AAO template by the flame synthesis technique (see Fig. 33). In the process, the Al film was not completely consumed during anodization and the Al film that remained between the AAO and Si substrate served as a buffer layer, resulting in smooth surface without cracks after the high temperature process. This demonstrated the feasibility for integration of carbon nanotube devices with Si integrated circuits.
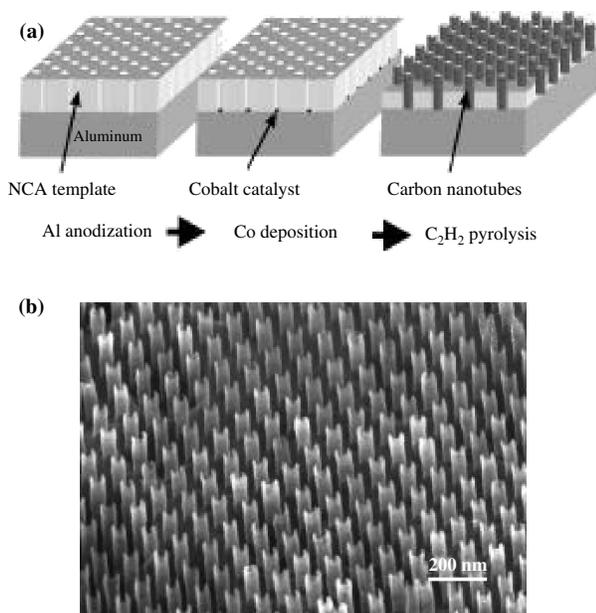
Figure 32. Schematic of fabrication process. (b) SEM image of the resulting hexagonally ordered array of carbon nanotubes fabricated using method in (a). Reprinted with permission from [236], J. Li et al., *Appl. Phys. Lett.* 75, 367 (1999). © 1999, American Institute of Physics.

7.2.2. Horizontally Aligned Carbon Nanotubes

The first horizontally aligned growth of carbon nanotubes was successfully carried out by Kroto's group at the University of Sussex, UK, and Cheetham' group at the University of California at Santa Barbara, USA [245]. The cobalt film deposited on a silica substrate was etched into tracks 1–20 μm wide using a laser beam. Laser beam generates tracks free of cobalt, leaving cobalt particles evenly positioned along the edges of the tracks. Carbon nanotube growth was carried out using pyrolysis of 2-amino-4,6-dichloro-*s*-triazine. After growth, dense nanotubes were found lying
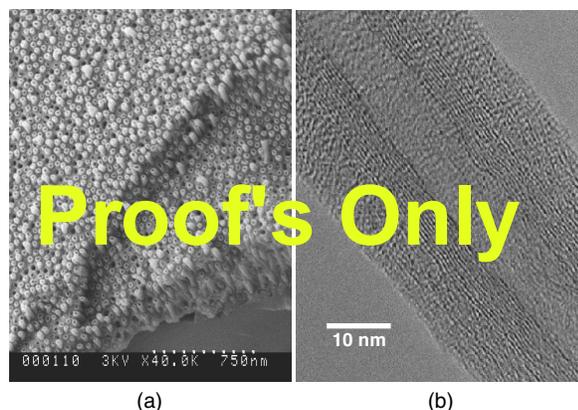
inside tracks and aligned from one edge to the other edge of a track [245]. This is the first synthesis of horizontally aligned nanotubes. Dai et al. [63, 141, 203, 246–253] continued extensive research on controllable growth of horizontally aligned carbon nanotubes on patterned Si substrates. A network of suspended SWNTs was grown from Si towers [249]. These suspended SWNTs might be used for interconnect of nanodevices. In order to enhance the directionality of growth, the electric field is introduced horizontally, resulting in better aligned growth of SWNTs as shown in Figure 34 [252]. This was also inspired by the field-assisted growth of vertically aligned CNTs [254]. It was suggested that the self-directed growth between the neighboring pillars is due to the swing of the nanotube cantilever which contacts a catalyst particle in liquid phase as the nanotube grows [255]. These results confirm the possibility of self-assembled wiring of nanostructures. MWNTs were grown from the cleaved side of a Si/SiO$_2$/Si mulitlayer structure to control the diameter of nanotubes [256]. In order for large-scale fabrication of nanodevices using CNTs, alternative selective placement of CNTs other than an AFM or STM is desirable. Controlled placement of SWNTs on prepatterned Si substrates has been achieved by a combination of the highly selective adsorption of SWNTs onto open regions of amino-functionalized SiO$_2$ in a polymer resist, followed by lift-off [257]. Controlled placement has also been achieved by electrical field-assisted alignment of CNTs under ac electric field [258]. Of particular interest is the utilization of nanotubes for nanolithography. One example is to use nanotubes as AFM tips to write nanopatterns [259]. Figure 35 shows the AFM image of a 10 nm wide line (SiO$_2$) fabricated by a nanotube tip [259]. Nanoelectrodes with a spacing of

Figure 33. (a) Cross-sectional SEM images of CNT arrays (about 500 nm long) on Si substrate fabricated in our laboratories. (b) TEM image of a CNT grown from the Al$_2$O$_3$ template showing multiwalls. Adapted with permission from [243], W. C. Hu et al., *J. Nanosci. Nanotechnol.* 2, 203 (2002). © 2002, American Scientific Publishers.
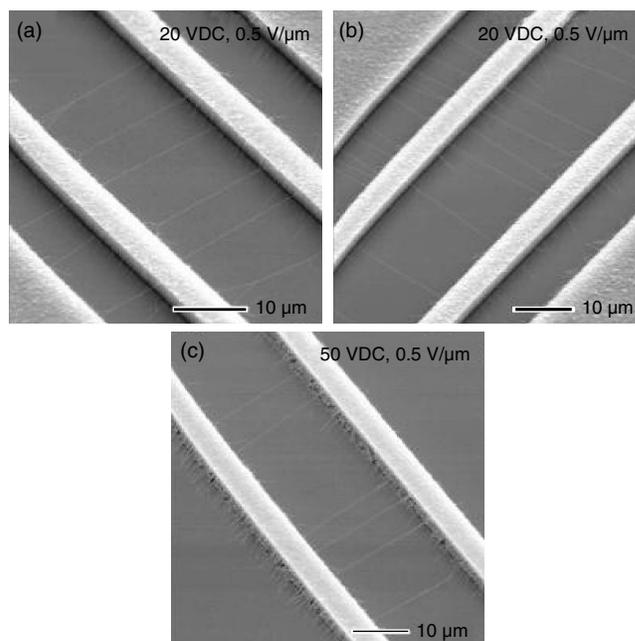

Figure 34. SEM images of suspended SWNTs grown in various electric fields. The spacing between the outer poly-Si electrodes is 40 μm in (a) and (b), and 100 μm in (c). Reprinted with permission from [252], Y. Zhang et al., *Appl. Phys. Lett.* 79, 3155 (2001). © 2001, American Institute of Physics.
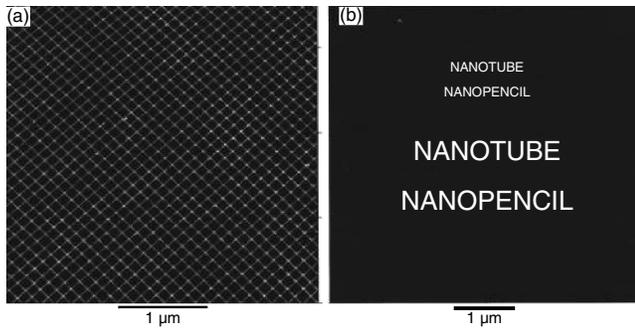
Figure 35. (a) AFM image of 2 nm tall, 10 mm wide, and 100 nm spaced silicon-oxide (light) lines fabricated by a nanotube tip. Bias voltage = −9 V; speed = 10 m/s; cantilever amplitude during lithography = 0.55 nm; cantilever amplitude = 9.6 nm. (b) Silicon oxide "words" written by the nanotube tip. Reprinted with permission from [259], H. Dai et al., *Appl. Phys. Lett.* 73, 1508 (1998). © 1998, American Institute of Physics.

~30 nm have been demonstrated using a carbon nanotube as a shadow mask, where a nanotube was suspended on PR supporters [260]. Figure 36 shows the schematic of the approach and Figure 37 shows the AFM image of the gold electrodes with a gap of ~30 nm [260]. Carbon nanotubes have also been used as masks for plasma etching where a ~20 nm nanowire beneath the nanotube was formed after etching [261].
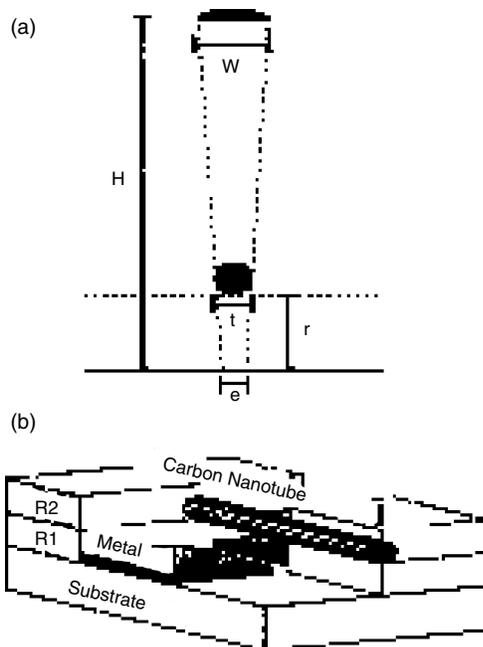

Figure 36. (a) In a shadow mask method, the shadow or gap size (ε) depends only on geometrical factors: the mask width or tube diameter (t), the tube–substrate distance (r), the evaporation source distance (H), and width (W). (b) Carbon nanotubes are incorporated between two layers of e-beam resist (R1 and R2) to act as a shadow mask preventing metal deposition at one point along a thin wire. The figure illustrates the process after metal deposition. Reprinted with permission from [260], J. Lefebvre et al., *Appl. Phys. Lett.* 76, 3828 (2000). © 2000, American Institute of Physics.
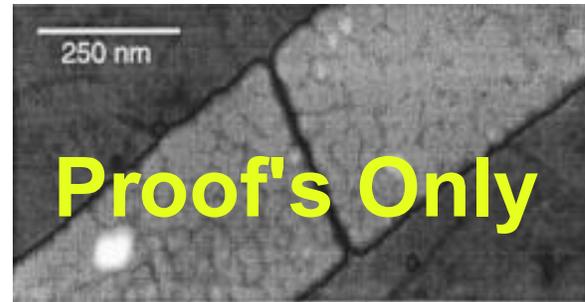

Figure 37. AFM image of a sub-30 nm gap in a 350 nm wide gold wire fabricated using a SWNT bundle. Individual SWNTs or small SWNT bundles (dark gray lines in the image) have been contacted using this method. Reprinted with permission from [260], J. Lefebvre et al., *Appl. Phys. Lett.* 76, 3828 (2000). © 2000, American Institute of Physics.

8. SUMMARY

Carbon nanotube-based nanoelectronics have been reviewed extensively, including electronic structure and transport properties of carbon nanotubes, various electronic devices, and nanotube-based nanofabrication. Since the discovery of CNTs for more than 10 years, great progress has been made in this field. Theoretical calculation predicted the one-dimensional energy band structure of single-wall carbon nanotubes with ballistic transport up to a few micrometers. Experiments successfully confirmed the theoretical predication. There have been demonstrations of the basic functions of carbon nanotube-based nanoelectronic devices such as single-electron transistors, field-effect transistors, logic gates, and memory devices. There is an almost limitless number of new geometries and topics waiting to be explored and all kinds of new structures to be created [262]. Upon comparison of their performance, carbon nanotube field-effect transistors are superior over Si MOS transistors. It is very promising to use carbon nanotube field-effect transistors as building blocks for large-scale integrated circuits when the current silicon technology reaches the end of its roadmap.

However, incorporation of the CNT devices to the existing Si manufacturing process is still far away. The current practice of fabrication of CNT transistors relies on arduous contacting of randomly distributed CNTs from suspension or time-consuming manipulation by AFM. Although great progress has been made in controllable growth and placement of carbon nanotubes, a planar process with high yield, which is the cornerstone of silicon technology, has not yet been achieved in the carbon nanotube process [263]. It is believed that in the next 10 to 20 years progress in process technologies for fabrication of carbon nanotube-based devices and circuits will eventually pave the way for electronics revolution in the molecular or nanoscale.

GLOSSARY

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